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This program began with the objective of develooping a novel optical interconnect technology that would provide parallel optical interconnections between electronic processing in a dynamically reconfigurable manner. The goal was to develop a switching fabric consisting of integrated optoelectronic switch arrays that offer a very compact, very-highinformation-throughout optical interconnect architecture. The technology we had chosen was based on the monolithic integration of VCSELs with other photonic and electronic technologies, including heterojunction HPTs and photothyristors, PIN and MSM photodiodes, and heterojunction bipolar HBTs. We have played a leading role in the development of monolithic OEIC technology based on VCSELs, as well as advancing the state-of-the-artin VCSEL technology itself.

We have developed an optical interconnect architecture and a high-speed OEIC switching technology that can provide reconfigurable interconnections between electronic processors, allowing then to communicate through a network of integrated optoelectronic transceivers and compact, monolithic space-division-multiplexed switches that provbide an optical link to other nodes and electrical access to each processor! These reconfigurable binary HPT/VCSEL switches can detect, regenerate and spatially reroute optical data, and can be programmed by simple voltages to perform different optical routing, fanout and logic functions. Arrays of switches with high optical gain were optically cascaded to form a multistage optical switching network that provide multipoint interconnections between nodes, through which multiple data channels can be routed in parallel without intermediate OE signal conversion. The functional capabilities of the reconfigurable optical switching fabric have been demonstrated at a data rate of >500 Mb/s.

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June 23, 1998

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Re: Grant # N00014-93-1-0852

Dear Dr. Park:

Enclosed please find three (3) copies of the SF 298 and final technical report for the grant referenced above. This report is submitted in accordance with the terms contained in Attachment Number 2 of the original grant document signed by Gail D. Boger, ONR Grants Officer on 6-21-93. Copies of this document are also provided to the other parties named in the report distribution list in Attachment Number 2, as amended 01 May 97.

The Principal Investigator for the University of New Mexico is Professor Julian Cheng. The title of the project is "High Speed Switches for Reconfigurable Optical Logic Arrays and Optical Interconnections".

If you have any questions regarding this report, please contact Professor Cheng at the address above.

Sincerely,

Roland Wildman
Unit Administrator

Enclosure

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1 - Prof. Cheng

FINAL REPORT

for

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Defense Advanced Research Projects Agency
and
The Office of Naval Research

Contract Period: **1 June, 1993 to 31 November, 1997**

Contract Title: **HIGH SPEED SWITCHES FOR RECONFIGURABLE OPTICAL LOGIC ARRAYS AND OPTICAL INTERCONNECTIONS**

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ABSTRACT

In this final report, we summarize our achievements under this DARPA research program, which began 1993 with the objective of developing a novel photonic switching technology that would combine the optical switching, routing, and logic functions, using a new class of cascadable optical/optoelectronic switching nodes that provide the basis for an intelligent, dynamically reconfigurable switching fabric with interfaces to electronics. We were seeking a role for optics that would encompass a broad spectrum of applications: from a passive, high performance optical bus or data link to an all-optical logic processor. Our goal is to show that optical technologies can perform more complex tasks: including dynamically reconfigurable multi-point networks that optically interconnect many electronic processors, and programmable optical logic arrays that execute complex optical logic sequences with a gate-level programmability. Our goal is to achieve *functional* flexibility by making the arrays spatially and functionally reconfigurable, so that they can be programmed to perform many different functions using the same hardware. With the emphasis on routing, these arrays can be used in a multi-channel packet-switch that spatially re-distributes parallel optical data packets to different destinations under either optical or electronic logic control. The goal is to develop a switching fabric consisting of integrated optoelectronic switch arrays that offer a very compact, very-high-information-throughput, optical interconnect architecture. When the emphasis is on logic, they can be used in a programmable optical logic array whose outputs are spatially reconfigured quickly to perform sequential logic operations using the same hardware.

The technology that we had chosen was based on the monolithic integration of vertical-cavity surface-emitting lasers (VCSELs) with other photonic and electronic technologies, including heterojunction photo-transistors (HPTs) and photothyristors (PNPNs), PIN and MSM photodiodes, and heterojunction bipolar transistors (HBTs). During the four years of this program, we have played a leading role in the development of monolithic optoelectronic integrated circuit (OEIC) technology based on VCSELs. The integration of VCSELs with other photonic and electronic components has produced novel optical and optoelectronic devices with a host of potential applications. Combining VCSELs with heterojunction phototransistors (HPTs) and photothyristors produced several families of high performance optical switches with alternatively latching, non-latching, or bistable switching characteristics, and with varying degrees of optical gain and contrast. Latching switches are useful for optical data storage and for performing logic operations, and a programmable optical logic gate array can perform many complex sequential optical logic functions. Non-latching optical switches integrating VCSELs and HPTs are particularly useful for optical switching and spatial routing operations.

One of the main applications of a reconfigurable optical interconnect technology is to link many electronic processors together to form an interactive network with a parallel processing capability. This calls for a dynamically reconfigurable interconnections that can route a large volume of digital data between many different computer processors and shared memory facilities, allowing them to communicate simultaneously in real time. We have developed a optical multi-access interconnect architecture and a high-speed OEIC switching technology that provide reconfigurable interconnections between electronic processors, allowing them to communicate through a network of integrated optoelectronic transceivers and compact, monolithic, space-division-multiplexed switches that provide an optical link to other nodes and electrical access to each processor.

The integrated optical routing switch arrays that we have developed can route many input optical data channels simultaneously to different optical output ports in a dynamically controllable manner. These reconfigurable binary HPT/VCSEL switches can detect, regenerate, and spatially re-route optical data, and can be programmed by simple voltages to perform different optical routing, fan-out, and logic functions. Arrays of switches with high optical gain were optically cascaded to form a multi-stage optical switching network that provide multi-point interconnections between nodes, through which multiple data channels can be routed in parallel without intermediate optoelectronic signal conversion. This programmable optical interconnect architecture can be used as a parallel, spatially-multiplexed, optical packet-switch. Most of the required functional capabilities of this reconfigurable optical switching fabric have been demonstrated at a data rate of >500 Mb/s, which exceeded the B-ISDN rate of 155 Mb/s, and the 622Mb/s target is easily within reach.

Smart pixels can be seen as parallel optical processing elements that perform a variety of functions on a two-dimensional array of input optical data to produce a logically and spatially modified, two-dimensional pattern of optical outputs. At one extreme, the smart pixel is a parallel optical link between intelligent electronic processing functions, where most if not all of the intelligence is vested in the electronic components. This is exemplified by the reconfigurable optical switching fabric described above. At the other extreme, the smart pixel can be an intelligent all-optical logic processor or optical computer. Individual smart pixel arrays can be monolithically integrated either as a space-invariant, single function logic array, or as a spatially inhomogeneous multi-functional optical logic circuit. Sequential smart pixel arrays can be optically cascaded to form a pipeline of distinct processing elements, or they can be configured as an optical programmable logic array (OPLA). In the course of this program, we have developed a programmable optical logic gate array technology, and demonstrated that individual logic arrays can be programmed to to perform different optical logic functions at speeds in excess of 100 Mb/s. Successive arrays can be optically cascaded to form a processing pipeline.

PART 1.

1. Technical Objective:

The objective of this program is to combine the optical switching, routing, and logic functions, using a new class of cascadable optical/optoelectronic switching nodes that provide the basis for an intelligent, dynamically reconfigurable switching fabric with interfaces to electronics. We seek a larger role for optics that encompasses a broad spectrum of applications: from a passive, high performance optical bus or data link to an all-optical logic processor. Our goal is to show that optical technologies can perform more complex tasks: including dynamically reconfigurable multi-point networks that optically interconnect many electronic processors, and programmable optical logic arrays that execute complex optical logic sequences with a gate-level programmability. Our goal is to achieve *functional* flexibility by making the arrays spatially and functionally reconfigurable, so that they can be programmed to perform many different functions using the same hardware. With the emphasis on routing, these arrays can be used in a multi-channel packet-switch that spatially re-distributes parallel optical data packets to different destinations under either optical or electronic logic control. When the emphasis is on logic, they can be used in a programmable optical logic array whose outputs are spatially reconfigured quickly to perform sequential logic operations using the same hardware.

2. Technical Approach:

Our technical approach is to integrate monolithic, two-dimensional arrays of emissive and photosensitive devices into arrays of optically-cascadable, multi-functional, optical/optoelectronic switching elements that perform a variety of parallel optical processing functions, including spatial switching and routing, logic, optoelectronic signal conversion, and optical amplification. The technology consists of a family of optical switches with alternatively non-latching, latching, or bistable switching characteristics, based on the monolithic integration of vertical-cavity surface-emitting lasers (VCSELs) with photosensitive components - such as heterojunction phototransistors (HPTs), photothyristors (PNPNs), or p-i-n photodiodes (PINs) - and with electronics, such as heterojunction bipolar transistor (HBT) technology. The technology development plan is as follows:

(1) Our first goal is to construct a simple optical analog of a transistor switch, which will perform switching and logic functions in a cascadable manner, using either optical or electrical input and output, while providing both electronic and optical gain.
(2) Combine these primary optical switches to form multi-functional switch nodes that can spatially reconfigure and thus re-route the optical signal paths, with a format that is substantially simpler and more compact than conventional optoelectronic integrated circuits (OEICs).
(3) Develop efficient, high speed optical switches by optimizing the technology for each of their constituents, including VCSELs, HPTs, and HBTs, and combining them using different functional configurations.
(4) Optimize the monolithic integration of VCSELs with HBT technology to form high-speed optoelectronic interfaces between VCSELs and VLSI electronics.
(5) Demonstrate a reconfigurable optical switching fabric with optoelectronic interfaces using these binary switch arrays.
(6) Demonstrate optically cascaded multi-stage switching and routing functions.
(7) Develop programmable optical logic functions using these optical switch arrays
(8) Demonstrate casacdable and programmable optical logic functions

3. Brief Summary of Accomplishments:

Our accomplishments are classified into the following five categories*:*

(1) Improve VCSEL performance by using novel structures or fabrication techniques, and improving our understanding of VCSEL physics:

(a) High-performance VCSELs were obtained by the continuous linear grading of the hetero-interfaces in its distributed Bragg reflector (DBR) mirrors, achieving a five-fold reduction in series resistance (<50Ω), an improved power efficiency (~10%), and lowering the *operating* voltages from 10V to <3V.

(b) Further improvements were made by selectively increasing the doping concentration of the DBR mirrors, while recreasing the bulk doping, which reduced the series resistance to <20Ω and the *operating* voltages to <2.5V, and produced even more thermally stable electrical characteristics.

(c) Using bi-parabolic compositional grading and selective, we have reduced the height of the hetero-barriers to a very low level without the use of higher doping, thereby reducing the operating voltages (1.75V threshold), power dissipation, and threshold current density (450 A/cm^2), while increasing the optical output power (15 mW), slope efficiency (>50%), and power conversion efficiency (22%, which is the highest value achieved by any λ=850 nm GaAs VCSEL). The resulting electrical characteristics are thermally very stable over a

wide temperature range from 80K to 400K, making it possible to design simpler laser drive circuits without requiring thermal compensation.

(d) Systematically studied the temperature dependence of VCSELs, and quantified the thermal de-tuning of the lasing mode and the gain peak. An optimized VCSEL can be designed to operate efficiently at any temperature range.

(e) By optimizing the alignment of the lasing mode with the gain, we have extended the temperature range for cw operation to a wider temperature range (90K-400K), with a maximum operating temperature of >400K for cw and >560K for pulse. The improved VCSEL has very low series resistance (12Ω), low operating voltages (1.8V at threshold and <2.5V at peak output), a very wide temperature range of operation (>500^{o}C pulsed, >300^{o}C cw), and stable cw electrical characteristics from 200K to 400K.

(f) Modeled (1993) the high speed performance of VCSELs, derived the equivalent circuit for high frequency modulation, clarified the roles of parasitics, mode-detuning, and gain limitations is curtailing the achievable bandwidth, which is estimated to be >44 Ghz (intrinsic).

(g) Demonstrated for the first time (1994) a high performance, inverted (n-side up) VCSEL structure grown epitaxially on a p-type substrate, with better lasing characteristics than the normal structures on n-GaAs.

(2) developed an optical/optoelectronic switch integrating the VCSEL with other photonic and electronic technologies; to improve the switch and to demonstrate its multi-functional capabilities:

(a) After several design variations using material grown by both MBE and MOCVD, we have achieved efficient HPTs with a maximum differential current gain of ~700, and a small-signal modulation bandwidth of ~3 GHz.

(b) Monolithically integrated *multi-functional* optical transceiver and optical switch using a three-terminal heterojunction phototransistors (3T-HPTs) and a VCSEL, demonstrated optical switching and optoelectronic signal conversion at >200 Mb/s (0.8 ns rise time). This switch can perform different combinations of electrical and optical switching to convert either electrical or optical input data into an optical or electrical format. Optical switching at 200 Mb/s, and optoelectronic conversion (*transmit or receive*) at a data rate of >500 Mb/s, have been demonstrated.

(c) By modifying the HBT design and using a self-aligned technology, we have improved its bandwidth to ~3 GHz, while achieving a sufficiently high current gain (~100). Demonstrated the high-speed, large-signal modulation of a monolithic HPT/VCSEL switch, with sub-nanosecond rise/fall times (~150 ps) for electrical switching, a rise time of a 0.8 ns for optical switching, and a small-signal modulation bandwidth of 4.2 GHz.

(d) Improved monolithic optical switch replacing the HPT with a p-i-n photodetector and a high-speed HBT. By separating the photodetection and gain functions, each component can be individually optimized to achieve higher gain (7) and a higher switching speed (>500 Mb/s).

(e) Demonstrated that the PIN/HBT/VCSEL switch can perform optical switching and optoelectronic signal conversion at a data rate of 100 Mb/s, while achieving a peak dc optical gain of 18 and an ac optical gain of 4.

(3) Designed an array of cascadable, dynamically reconfigurable, multi-functional binary optical switches:

(a) Designed monolithic, 1x2 and 2x2 binary optical switches integrating VCSELs and HPTs, which can be programmed to perform different optical routing operations, including bypass or exchange. These switches permit input optical data to be spatially routed to different output ports in a parallel and reconfigurable manner, and with an optical fan-out. Experimentally demonstrated optical routing at 20 Mb/s.

(b) Designed an improved HPT/VCSEL switch that can be switched both electrically and optically using and VCSELs and three-terminal HPTs. Electrical inputs can modulate the switch to produce an optical output, and optical inputs can modulate the switch to produce an electrical output, both of which can be spatially routed. Demonstrated optical switching with a risetime of ~ 3 ns, and electrically gain-switching at 1 Gb/s rate to produce optical pulses with a 56 ps rise time and <100 ps pulsewidth.

(c) Designed binary 3T-HPT/VCSEL routing switch arrays that can perform optical switching and routing, as well as the transmit and receive functions, demonstrating large-signal modulation by 200 Mb/s optical data, and by 500 Mb/s *electrical* input data.

(d) Improved switching function by separating the light detection and amplification functions using a binary PIN/HBT/VCSEL switch, which reconciles the conflicting requirements of high current gain, high coupling efficiency, and high speed that had limited the performance of the HPT/VCSEL switch. A new generation of binary routing switches with higher optical switching speed (500 Mb/s) and higher optical gain (7) have been demonstrated.

(d) Using new PIN/HBT/VCSEL switches with a high optical gain, we demonstrated the *cascaded, multi-stage* operation of two arrays of *binary optical switches* each integrating an array of PINs and HBTs with an array of VCSELs. Individual binary PIN/HBT/VCSEL switches have achieved a peak dc optical gain of 18 and an ac optical gain of 4 at 50 Mb/s. Optically-cascaded, two-stage switching operation has been demonstrated, with an overall cascaded dc optical gain of 50 and an ac gain of 8, and a data rate of 100 Mb/s.

(e) Experimentally demonstrated the optical switching and routing operations at 500 Mb/s, using binary PIN/HBT/VCSEL switches modulated by electrical or optical input data.

(4) Integrating VCSELs with GaAs HBT electronics technology:

(a) Monolithic integration of a VCSEL with a HBT to form an optoelectronic interface that provides electrical access between the HPT/VCSEL switching fabric and its external electronic control or data I/O functions.

(b) Demonstrated the efficient conversion of electrical input data to optical data by an optoelectronic HBT/VCSEL interface, with high current gain (>500), a high conversion efficiency (150 mW/mA), and low base current (7μA at threshold), and a 3 dB bandwidth of ~200 Mhz.

(c) Developed high speed HBTs (20 Ghz bandwidth) for integration with VCSEL.

(c) Measured and modeled the high frequency modulation characteristics of a HBT/VCSEL switch, demonstrated large-signal modulation at >500Mb/s, a small-signal modulation bandwidth of 4.2 GHz, and an optical signal rise time of < 0.6ns.

(5) Programmable optical gate arrays and experimental demonstration of a cascaded multi-stage optical switching network.

(a) Fabricated a linear array of binary HPT/VCSEL *optical* switches that can be reconfigured at the gate level to perform different Boolean optical logic operations (AND or OR) at a data rate of >20 Mb/s, with an optical fan-out of up to 2.

(b) Fabricated linear, cascadable, 1x4 and 1x8 arrays of PIN/HBT/VCSEL with optoelectronic (O/E) interfaces, and experimentally demonstrated switching and at 500 Mb/s, with a single-stage optical gain of 7.5 dB. In the new design, every PIN/HBT/VCSEL switch contains its own independently-addressable electrical input terminal. The HBTs have a dc current gain of 70-90, and a 3-dB modulation bandwidth of 550 MHz, which gives rise to a large-signal rise-time (10%-90%) of 630 ps.

(c) Using the PIN/HBT/VCSEL switches as transceivers, demonstrated optical transmission through single-mode and multi-mode fibers with link distances of up to 1 km and at data rates up to 1 Gb/s. Multi-mode transmission at 650 Mb/s was achieved with a bit-error-rate of $<1\times10^{-9}$ with a sensitivity of -12 dBm, and at 1 Gb/s with a sensitivity of -4 dBm.

(c) Improved logic performance, including a high optical gain (7), a higher data rate (~100 Mb/s), and electrical access (electrical logic inputs or outputs), has been by a programmable optical logic gate array consisting of integrated PIN/HBT/VCSEL binary switches that can be dynamically reconfigured at the gate level to perform different logic functions. Demonstrated programmable optical logic functions (e.g., AND or OR) at selected nodes at 100 Mb/s, using either optical or electrical logic inputs. The arrays are dynamically programmable at the gate level to perform different logic operations, and to spatially re-route the optical logic outputs (with a selectable fan-out) to provide the inputs for the next array, from one clock cycle to the next.

(d) Designed an optical programmable logic gate array (OPLA), which consists of an array of binary PIN/HBT input nodes and a monolithic array of VCSEL output nodes. Each is reconfigured after each step of the process sequence to control the optical routing, optical logic, and fan-out at the gate level. We have demonstrated high speed programmable optical logic at a data rate of 100 Mb/s, using either electrical or optical inputs. Complex logic functions have been demonstrated by optically cascading two OPLAs, and programming the functions of each node at the gate level. Rise and fall times of ~5 ns, and a switching energy of ~300 fJ, have been achieved.

4. Significance of This Work:

This versatile optical switching technology, which is monolithically integrable in a surface-normal, 2-dimensional format, provides a dense array of optical switches and interconnections. The switches in each array can be programmed to select different optical input-output paths, while a multi-stage network of these switch arrays can simultaneously route a multitude of optical input signals to different output ports in a dynamically reconfigurable manner through spatially multiplexed switching operations. They can thus implement a multi-channel optical routing switch, a board-to-board interconnection network linking distributed computer processors, or a self-routing ATM (asynchronous transfer mode) packet switch, operating at a gigabit-per-sec data rate. Each switch provides optical routing as well as an optical-to-electronic interfaces. As interactive computer networks grow in importance, and the demand for multi-media services on the information highway continues its inexorable growth, the need for ever-greater bandwidth and multiple access will inevitably make a reconfigurable, parallel optical data link a necessity.

5. Participants:

Principal Investigator: Julian Cheng

Graduate students: Bo Lu, Yin-Chen Lu, Geraldo Ortiz, Drew Alduino, and C. Hains

Collaborators:

Sandia National Labs:

Dr. R. P. Schneider, Dr. M. J. Hafich, Dr. John Zolper

PART 2. Detailed Discussion of this Program and a Summary of its Accomplishments:

1. Introduction

For short-distance data networking applications, there is a growing need for parallel optical links and high-speed, multiple-access buses to alleviate the input/output bottleneck in data communication. In the past, the insertion of photonic technology into the data communication market has occurred only in the form of simple point-to-point optical data links that required no reconfiguration. But as computers improve in speed and processing capacity, and are increasingly being linked together in to form interactive, shared facility networks, the increased demand for data communication requires new interconnect paradigms that provide real-time, parallel data transfer at increasingly higher data rates. The focus will shift from single-access, point-to-point optical links towards more flexible multiple-access networks that can route a vast amount of information simultaneously and interchangeably between a large number of nodes via rapidly reconfigurable interconnections. This involves not only the transmission, but also the switching and routing of optical data. In this program, we have designed a new, dynamically reconfigurable optical interconnect technology that addresses the requirements of future computer networks, and we have developed an enabling switching technology based on the integration of vertical-cavity surface-emitting lasers (VCSELs) with other photonic and electronic component technologies.

Traditionally, switching can be performed at lower frequencies in the electronic domain through electronic crossbars and bus switches, which are limited in both speed (< 100 Mb/s) and in switching matrix size. As the processor speed and data throughput both continue to increase, it will become increasingly difficult to produce the switching networks needed for routing a large number of data channels. With the processor speed already surpassing 250 MHz, and the data width rapidly moving towards 64 bits and beyond, parallel and high-speed data buses are needed to support the peak processor performance without intermediate multiplexing and demultiplexing (MUX/DEMUX) operations. But at higher speeds and/or larger transmission distances, the communication between the nodes becomes increasingly dominated by latency, timing skew, and power dissipation, which can be reduced by replacing the electrical interconnection with an optical fabric. This provided the motivation for our research in photonic switching networks that would allow many parallel data channels to be routed simultaneously in the optical domain. Since data is transmitted between distant nodes in an optical format, there is electrical isolation between successive stages.

Dynamically reconfigurable optical switching networks are useful for a variety of applications in parallel optical processing. They have important applications in future high speed computer systems, where large numbers of individual processors will be linked together to form interactive, shared-facility networks with the enhanced computational power of a supercomputer. They may be used to interconnect a large number of boards in the backplane of a parallel multi-processor network, which can be programmed rapidly in real time to perform multiple tasks in parallel. Alternatively, they may also be used to interconnect a network of interactive computers that are distributed across distant spatial locations, where the larger distances and higher speeds involved make an optical link imperative. Individual processors must have multiple access to the optical network in order to facilitate the simultaneous communication between many different processors. The flexible, monolithic optoelectronic technology that we have developed can optically interconnect a network of local or distributed

computer processors. These high-speed electronic processors may reside as multi-chip-modules (MCMs) on different boards, each of which contains an array of optoelectronic routing switches that provide access to an optical network, whose total data capacity may reach tens of Gb/s.

Since data communication generally tends to be bursty in nature, the optical interconnect architecture must be able to dynamically re-route many sources of packetized optical data simultaneously through different channels. In addition to being a densely parallel optical link, reconfigurability is needed to facilitate the intelligent routing of data packets. These packets may be transmitted through an interactive optical network with a local self-routing capability, or the connections may be programmed in a centralized fashion by a host computer.

During the course of this program, much work was also done to improve the performance of VCSEL technology, which had provided us with an early lead in achieving many different high performance optoelectronic device technologies based on VCSELs. These included several families of optical switches with alternatively latching, non-latching, or bistable characteristics, monolithic optical logic gates and logic families, reconfigurable optical routing switches, programmable optical logic gates, high-speed optical transceivers, an optically cascaded multi-stage switching fabric, and a programmable optical logic gate array.

In the first phase of this program, we had developed the enabling technology for a high-speed optoelectronic switching fabric. The technology consisted of monolithic arrays of surface-normal binary optical switches based on the monolithic integration of heterojunction phototransistors (HPTs) with vertical-cavity surface-emitting lasers (VCSELs). Each switch node contains a HPT, which provided an optical input port, optoelectronic signal conversion, and electronic gain, and a VCSEL that provided the optical output. The HPT/VCSEL switch is a regenerative optical device that amplifies the input optical signal to produce a larger optical output. By interconnecting pairs of these switching nodes in a specific manner, optical bypass-exchange switching operation was achieved. The input optical data channels were routed in either a straight-through (bypass) or crossed-over (exchange) mode in response to simple routing control voltages. Reconfiguration occurred at a speed approaching the switching speed of an HPT/VCSEL switch, although that is not necessary for the routing of optical data packets. Each binary switch thus provides an optical-to-optical interface for optical communication between processors, as well as O/E and E/O interfaces to electronics, and it also performs the optical routing functions. A large number of HPT/VCSEL switches can be readily integrated on a single chip, which provides a large and compact routing matrix with relatively short electrical signal path lengths. At the system level, we have used these reconfigurable routing switch arrays to demonstrate a novel and dynamically reconfigurable, multi-stage optical interconnection network.

Our approach to a reconfigurable photonic switching network is based on space-division multiplexing (SDM), which allows a large number of optical data channels to be routed to different destinations in parallel using two dimensional optical switch arrays. The usefulness of this optical interconnect is greatly enhanced by the fact that all the routing paths are dynamically reconfigurable, and the network is flexible enough to permit one-to-one, broadcast, or multi-cast operation. We will summarize our accomplishments for this program in detail below.

2. Detailed Summary of Program Achievements:

2.1. Development of High-Performance VCSEL Technology:

VCSELs are ideally suited for parallel optical interconnect applications since they are readily integrated into dense, two-dimensional arrays to provide a compact, parallel, surface-nomal architecture. The VCSEL provides a high speed optical source with good optical beam quality, high output power, low power dissipation, good thermal stability, stable current-voltage characteristics, and a very wide operating temperature range. Much of our work on switching requires the achievement of high performance VCSELs, and a significant amount of work was done to improve their characteristics, including their modulation speed (~10 GHz measured bandwidth, 45 Ghz intrinsic), their thermal stability (<3 dB variation in threshold over a temperature range 150°C wide), and more importantly for switching, their slope efficiency (45%), power conversion efficiency (22%) and their integrability with other technologies (VCSELs on both p-type and n-type, as well as on semi-insulating substrates). We have fabricated two types of VCSELs, whose active areas are defined by proton implantation (upper) and oxide confinement (lower), respectively. The typical characteristics a of 16 μm diameter proton-implanted device used in this research are shown in fig. 1, while those of an oxide-confined device are shown in fig. 2.

Our first major contribution to VCSEL technology was to demonstrate that the VCSEL's electrical characteristics can be greatly improved by the continuous compositional grading and selective doping of the heterointerfaces by using MOCVD. This reduced the barrier resistivity to a level approaching that of barrier-free bulk transport, and for the first time, we had dropped the operating voltages of VCSELs from 5-10 V down to 2 V, and the series resistance from 300 Ω to less than 50 Ω (1991-92). It would be two years before other group would achieve these results. We also showed that the temperature dependent behavior of VCSELs is strongly limited by the roll-over of its lasing characteristics resulting from the thermally-induced de-tuning of the lasing mode with respect to the gain peak (1993), which curtailed its temperature range of operation. By aligning the cavity mode to the gain peak, power dissipation is reduced, allowing the resulting VCSELs to to achieve very stable current-voltage characteristics and stable lasing operation over a wider range of temperature (100K to 580K pulsed, 100K to 410K cw). This relaxed the need for thermally-compensated drive ciruits and alleviated the thermal management issues. VCSELs with lasing wavelength variations of less than 1% across a 2" wafer was also achieved.

From our detailed high-speed modeling and experimental and work on VCSELs, we have clarified the intrinsic and extrinsic effects that governed their modulation response (intrinsic $f_{max} \cong 44$ Ghz). We have also carried out optical fiber transmission experiments at a data rate of up to 1 Gb/s, using a VCSEL-based transmitter and both single-mode and multi-mode fibers. Figure 3 shows a wide open eye diagram at a signal level of -20 dBm, with a bit-error rate of better than 10^{-13} for the latter, and about 10^{-10} for the former, which was limited by dispersion and mode-selective loss. We were also the first to achieve an inverted VCSEL structure grown on a p-type GaAs substrate (1993), which is advantageous from the perspective of achieving faster electronic drive circuits (by using silicon npn-transistors) or for optoelectronic integration), see fig. 4.

2.2. A Spatially-Multiplexed, Dynamically Reconfigurable Optical Interconnect Architecture

An optically regenerative, surface-normal photonic switch that provides optical amplification as well as two-dimensional access could result in a compact and more densely-packed monolithic architecture. By optically cascading these switching arrays, a very compact, multi-stage, optical interconnection network can be realized. Figure 5 shows a reconfigurable optical architecture that illustrates many of the functions that may be required in a highly-parallel optical processor, in which parallelism takes on the form of two-dimensional arrays. Different array technologies are needed to perform the various functions in the optical domain, including: optical data generation, amplification, and detection, optical logic or other digital signal processing functions, optical data storage. But most importantly, dynamical reconfiguration of the optical data paths is needed to allow these arrays to perform different functions using the same hardware, thereby providing the processor with the kind of programmability that is similar to an electronic programmable logic gate array. When the emphasis is on reconfiguration, the array processor functions as a programmable optical routing switch. When logic is emphasized, however, the processor becomes a programmable optical computer or digital signal processor.

An important application for this optical switching fabric is that of a reconfigurable optical network interconnecting a large number of electronic processors consisting of mutli-chip modules (MCMs) residing on the same board or on different boards (figure 6). Electronic processors currently communicate with processors on other boards via parallel electronic data buses. With increasing processing speeds or larger transmission distances, the communication between boards becomes increasingly dominated by latency, timing skew, and power dissipation, which can be reduced by replacing the electrical interconnection with an optical one, using fiber or free space as the transmission medium. In addition to providing optical interconnections between successive processing stages, the switching fabric also provides optical-to-electronic (O/E and E/O) interfaces to VLSI electronics. At each end of the optical link is an electrical-to optical (E/O) or optical-to-electrical (O/E) interface that converts data between its electrical and optical formats. For simple parallel optical interconnects, these interfaces mostly consist of optical transmitter and receiver arrays that provided fixed paths between selected processors. As larger numbers of high-speed computer processors are linked together to form interactive networks with a parallel processing capability, there is a need for real-time, parallel communication between different processors at increasingly higher data rates. This requires an optical interconnection network that provides dynamically reconfigurable connections between nodes, and which can support a larger switching matrix size while providing higher speed and optical isolation between stages.

Our approach to a large-scale multi-processor interconnect is based on the dynamic reconfiguration of a multi-stage, multi-path, space-division-multipled optical routing network (figure 6). Space-division-multiple access (SDMA) networks can provide a very large spatial bandwidth since large, compact switching matrices can be achieved by optoelectronic integration, and many parallel channels can be routed simultaneously through space. By arranging the network in the form of a closed ring, any node can be interconnected to another by selecting a routing path through the switching fabric with a small number of intermediate hops. Figure 7 shows a *dynamically reconfigurable optical interconnection architecture* for optically linking electronic processors together and routing data through parallel optical channels. A network of optoelectronic switches provide optical links between nodes and electrical access (an electrical $\Leftrightarrow$ optical interface) to each processor. Each node must be able to transmit or receive optical data, or to re-route it optically to the next stage (routing or optical bypass mode). The received optical data (P_{in}) is converted into electrical data (E_{out}), which is

either *dropped* at that node, or is *regenerated optically* and routed to the next stage (P_{out}). The switch must also accept electrical input data (E_{in}) from a local processor and convert it to an optical format (P_{out}) for transmission. To perform the transceiver functions, each switch must provide an optical source and photodetector, as well as their drive circuitry and the switching functions, and it must be able to convert digital data between various electrical and optical input/output formats.

Figure 7a shows a 4-stage Banyan network that provides complete connectivity between 64 processors distributed into 4 clusters, each with 16 nodes. Each node can transmit data to other nodes through one or more intermediate hops, using optical signal paths that can be individually programmed. The signals are optically cascaded between stages until they reach their destinations, where they are converted back into electrical data. The switching fabric consists of 4 monolithic arrays of optoelectronic switches, each with 16 optical input and output ports, and each switch node is capable of performing either the optical switching or optoelectronic signal conversion functions. The example of a 1x8 linear HPT/VCSEL switch array is shown schematically in figure 7b, and the optical switching and optoelectronic conversion functions of a 2x2 multiprocessor interconnection network are illustrated in figure 7c. Each node is connected to a shared optical transmission medium (free space or fiber), with which it interacts by transmitting, receiving, or optically bypassing optical data. The compact monolithic switch arrays contain very short electrical routing paths, while their optical outputs can be projected across signficant physical distances.

Figure 7c also shows a simplified two-stage optical interconnection network that illustrates the communication of data between four N-bit processors residing on two different boards. Each board also contains one stage of a 2x2 optoelectronic switching matrix, with two nodes per stage, each of which is electrically connected to a processor (only one bit is shown). Each switch node can be activated by either an optical or electrical input, and produces either an optical or electrical output. Each node can be modulated, either by an optical input from another node or by an electrical input from its associated processor, to produce a current modulation that is spatially routed to one or more nodes within the switch array, where it produces both a modulated electrical signal that is sent to the corresponding processor and a regenerated optical output that is optically transmitted to the next stage. The internal routing paths within each array can be reconfigured by setting the control voltages. Parallel optical data channels propagate between boards through free space or through a weakly-guided medium, and are routed to other nodes in successive stages under electronic routing control. Local or centralized routing control can be used, and both packet and circuit switching are possible.

2.3. The Achievement of a Reconfigurable Switching Technology

2.3.a. Optical Switches Based on the Integration of VCSELS with HPTs and PNPNs

The integration of VCSELs with other photonic and electronic components produced novel optical and optoelectronic devices with a host of potential applications. Integrating VCSELs with heterojunction phototransistors (HPTs) and photothyristors (figure 8) produced several families of high performance optical switches with alternatively latching, non-latching, or bistable switching characteristics (figure 8). These switches possess greatly varying degrees of optical gain and contrast, as well as an adjustable switching threshold. Latching switches are useful for optical data storage and for performing optical logic operations, and a programmable optical logic gate array has been made that can perform many complex sequential optical logic

functions. Non-latching optical switches integrating VCSELs and HPTs form the technology base for the optical switching and spatial routing operations.

2.3.b. Reconfigurable Binary Optical Routing Switches

Reconfigurable spatial routing of optical data packets can be achieved by using a simple, binary optical routing switch consisting of a two-segment HPT, each of which is connected to a different VCSEL. The VCSEL and HPT epilayers are monolithically integrated on the same GaAs substrate (figure 9). By segmenting the HPT into two contiguous but electrically-isolated segments that share a common optical input, and connecting each segment to a different VCSEL output port, reconfigurable spatial routing of the input optical data can be achieved by independently controlling the bias voltages of each HPT/VCSEL pair. Figure 10 shows the design and optical routing functions of a binary 1x2 switch. By controlling the voltages V_1 and V_2, packets of optical data impinging on the HPT generate an amplified photocurrents I_c that modulates the VCSELs independently to produce optically regenerated outputs that emerge from either, neither, or both (fan-out of 2) of the output ports. Electrical routing within each stage is limited to very short distances within a compact two-dimensional array of switch nodes. The routing paths and optical fan-out are controlled by the voltages V_1 and V_2, as demonstrated experimentally in Fig. 10. Arrays of 1x2 switches form each stage of the multi-stage shuffle network that is depicted in figure 6, and all the connections can be dynamically reconfigured using the routing control voltages.

The 2x2 optical bypass-exchange switch (figure 11) consists of two 1x2 switch nodes pairing the same two input and output channels. Arrays of 2x2 switches may be used to implement routing networks with a Banyan topology. Routing is controlled by two pairs of voltages - (V_1, V_2) and (V_2', V_1') - which select the bypass or exchange mode of the switch. These optical switching functions are experimentally demonstrated in figure 11. As the routing control voltages are toggled between the two inner and outer switch connections, the optically regenerated pulses of the two input data channels emerge alternately from the same or opposite output ports (VCSELs).

In 1993, both 1x2 (figure 10) and 2x2 (figure 11) versions of this HPT/VCSEL switch were Later (1995), the optical switching speed was increased by an order of magnitude to 200 Mb/s using an improved switch design.

The reconfigurable binary HPT/VCSEL switches can detect, regenerate, and spatially re-route optical data in a programmable manner. The multi-functional capability of these binary switches is illustrated in Fig. 12, which shows that a single array of these switches can be programmed by simple voltages to perform different optical routing, fan-out, and logic functions. Arrays of these switches can be cascaded to form a multi-stage optical switching network that routes data through parallel optical channels to provide multi-point interconnections between nodes. These interconnections can be dynamically reconfigured, thus providing a useful platform for a parallel, spatially-multiplexed packet switch or a multi-processor interconnect.

2.3.c. Optoelectronic Integration of VCSELS with HBT Technology

The integration of VCSELs with high speed electronics is driven by: 1) the desire to combine the optical source array and its driver circuits into a single technology, and 2) to provide a simple optoelectronic interface for VCSEL-based photonic switching networks. Before the electronic processing elements can communicate with each other through parallel optical

channels, an optoelectronic interface is needed to effect electrical ⇔ optical signal conversion. This interface must perform the functions of an optical transceiver, allowing the switch to communicate with a processor or its electronic control functions. The integration of VCSELs with heterojunction bipolar transistor (HBT) technology is favored by the compatibility of their epitaxial structures, operating current densities, physical sizes, and modulation speeds.

The simplest VCSEL drive circuit is an HBT/VCSEL optoelectronic switch in an emitter-follower configuration, which is mandated by the common n-substrate contact of the VCSELs. A common-emitter configuration would be more suitable, and allows more flexible connections to be made among devices, but this requires that the VCSELs be grown on a p-type or a semi-insulating substrate. In 1992, we achieved the first monolithic optoelectronic switch integrating a VCSEL with a GaAs/AlGaAs HBT (figure 13), with a high current gain (β~500) and a large electrical-to-optical conversion efficiency (150 mW/mA), but high speed switching performance was limited to a small-signal bandwidth of ≈100 Mhz (≈50 Mb/s).

Figure 13 shows an integrated HBT/VCSEL switch with a 15x15μm^2 emitter area and a VCSEL active area diameter of 20μm. The HBT saturates at <1 V, while the VCSEL threshold voltage is 2.0 V, and switching can be effected with a collector bias of less than 3V. The relative small-signal response of I_c to a voltage modulation applied to the base is shown in Fig. 14, which shows the forward transmission coefficient S_{21}, and the current gain h_{21}. The HBT has a unity-gain bandwidth of 500MHz, with a corresponding time constant τ=0.32ns. Figure 14c shows the small-signal electrical-to-optical modulation response of the switch at different values of bias current, which has the typical resonant frequency response of a diode laser modulated above threshold, modified by the transconductance of the follower circuit. The modulation response saturates at a bandwidth of f_{max} ~4GHz.

Figure 14b shows the eye diagrams of this HBT/VCSEL switch under 500Mb/s, large-signal pseudorandom data modulation. The upper trace represents the modulated light output of the VCSEL, while the lower trace shows the modulated collector current I_c. The modulated electrical pulses have a 10%-90% transition time (~2.2τ) of 0.6ns, and shows no significant pulse narrowing due to a turn-on delay when the switch is pre-biased above the lasing threshold. The same epitaxial structure can also be used for the integration of VCSELs with more complex HBT electronic logic and interface circuits, or with phototransistors to perform the optical switching functions. Arrays of such switches form a compact optoelectronic interface for a parallel optical data link.

2.3.d. Integrated 3-Terminal HPT/VCSEL Switch with an Optoelectronic Interface

High performance optical and optoelectronic switches with high gain and contrast, and moderately low optical switching energies have been made by integrating the VCSEL with an HPT. As we have seen (figures 9-11) these switches have been combined into binary configurations to perform different spatial routing functions, such as the bypass and exchange of optical signals, under simple voltage control, but an electrical interface was lacking. Using a three-terminal HPT/VCSEL optical switching technology, we have shown that the functions of the HPT and the HBT can be combined in a single switch (fig. 15), thereby integrating both the optical switching and optoelectronic signal conversion (interface) functions. These *multi-functional* switches can perform different combinations of electrical and optical switching at high data rates, and it can combine electrical and optical data packets into a common format.

By replacing each of the two-terminal HPTs in a binary optical routing switch with a three-terminal(3T)-HPT, and adding the electrical input and output ports, these spatial routing switches can perform the simplified transceiver functions. Figure 15(a,c) shows an integrated switch consisting of a three-terminal heterojunction phototransistor and a VCSEL. The switch can be activated by either an optical signal (P_{in}) from another node or by the electrical input (E_{in}) from a local processor, producing a switched optical output (P_{out}) from the VCSEL that is transmitted to the next node, as well as a modulated collector current (I_c) and an output voltage (E_{out}) that is coupled to an electronic processor in the cluster (figure 15b). The phototransistor base terminal serves as an electrical input port for both data and prebias, and the operating characteristics of the switch can be adjusted using the latter. For example, the switch can be prebiased near the lasing threshold of the VCSEL to minimize the optical power needed to effect switching. Each node can either receive or transmit optical data, or optically re-route it to other nodes in the optical switching network. The optical response of P_{out} to a voltage E_{in} applied to the base of the HPT represents the transmitter function, while the response of E_{out} to an optical input P_{in} incident on the HPT represents the receiver function. The production of an *optically switched* and *optically regenerated* output P_{out} in response to P_{in} represents the optical bypass or routing function.

The optical input P_{in} illuminates an area lying between the emitter and base contacts (figure 15c), and the quantum efficiency of the HPT is ≈65%. The various switching functions are demonstrated experimentally using a combination of optical and electrical inputs, and the results are shown in Fig. 15d. Two different data patterns modulate the optical and electrical inputs to the HPT during alternate, non-overlapping time intervals. The optical input P_{in} is incident on the base-collector junction of the HPT, while the electrical data E_{in} directly modulates the base of the HPT, each at a data rate of 200 Mb/s. The switch converted the electrical and optical input data packets into switched optical and electrical outputs, which were combined into a single data stream. The first two traces in Fig. 15d show the modulated collector current I_c in the presence of *only* the electrical (trace 1) or optical (trace 2) input data. Traces 3 and 4 show the modulated electrical output (I_c) and optical output (P_{out}) when the optical and electrical input data are both present, which contain replicas of both the optical and electrical inputs, thus showing the conversion of P_{in} and E_{in} into a switched optical or electrical format. Trace 3 demonstrates electrical switching and optoelectronic data conversion (receiver function), while trace 4 demonstrates optical switching and optoelectronic data conversion (transmitter function). Electrical input data E_{in} likewise produces a modulated output current and an optical output.

The large-signal modulation characteristics of the switch are depicted in Figure 15e. The eye-diagrams represent the optical response P_{out} (lower traces) and the electrical response E_{out} (upper traces) of the switch to large-signal modulation by pseudorandom optical data P_{in} (left) and electrical data E_{in} (right) at 200 Mb/s. The 10%-90% rise time of each pulse is 0.8 ns. Integrated HBT/VCSEL driver circuits with a data rate of ~1 Gb/s appear to be within reach.

2.3.e. High-Speed Optical Switching and Routing using a new Array Design:

In order to improve the performance of the binary optical switch based on the 3T-HPT design, the switching fabric was redesigned using linear arrays of individually-addressable binary HBT/PIN/VCSEL switches integrating HBTs, p-i-n photodiodes, and VCSELs. Separating the 3T-HPT into two different entities - a p-i-n photodiode (PIN) for photodetection and a heterojunction bipolar transistor (HBT) for gain - allows each component to be individually

optimized to achieve higher gain and a higher switching speed. In the new switch design (figure 16a,b,c) each node contains its own independently-addressable electrical input terminal. In addition, the input ports were re-designed so that the PIN pairs have an improved response time and a higher optical coupling efficiency. To improve switching speed, the HBTs have also been redesigned to have a smaller base-emitter junction and a lower base resistance. Arrays of 1x4 and 1x8 switches were fabricated and were used in parallel optical switching experiments. A cascadable binary optical routing switch with improved switching performance was thus realized.

High-speed electrical and optical switching, as well as the reconfigurable routing of optical signals, have been demonstrated at high speed (400-500 Mb/s), with an high optical gain of 7.5 dB, which is essential for cascaded switching operation. The HBTs used in these experiments have a dc current gain of 90, a 3-dB modulation bandwidth of 550 MHz, a rise-time (10%-90%) of 630 ps. The VCSELs has a high slope efficiency of 35%. The switches were pre-biased near the VCSELs' lasing threshold to minimize the turn-on delay.

Figure 16d demonstrates the conversion of a large-amplitude electrical input signal into a switched optical output. The 400 Mb/s NRZ electrical input data is applied to the base of the HBT. Figure 16e demonstrates the optical-to-optical switching performance of the binary switch. The input optical data impinged upon the segmented PIN pair, producing amplified photocurrent pulses that modulate the VCSEL from below threshold to an optical output level of ~1 mW. Fig. 16f demonstrates optical routing and fan-out using the binary optical switch. The same optical input signal was coupled equally into the PIN pair, with the switch pre-biased near lasing threshold. When a bias voltage was applied to the collector of each PIN/HBT/VCSEL circuit, a single optical input signal was routed to each of the two optical output ports, modulating each VCSEL at a data rate of 500 Mb/s. Biasing only one of the circuits results in routing of the optical data to one output port or the other.

In order to optically cascade these switches in a multi-stage routing or interconnection network, each switch must possess sufficient optical gain to compensate for the optical losses incurred in coupling and transmission. The optical gain depends on the optical coupling efficiency (~18%), the PIN quantum efficiency (39%), the current gain of the HBT (90), and the slope efficiency of the VCSEL (35%). An optical gain of 7.5 dB was achieved using these switches. An improved version of the HBT/PIN/VCSEL switch based on a common p-substrate configuration is shown in figure 17.

2.3.f. Optically-Cascaded Multi-Stage Switching Operation and Reconfigurable Multi-Point Optical Interconnects:

Reconfigurable routing between a large number of node can be achieved using a mutli-stage optical routing network in which each stage contains an array of binary optical routing switches (fig. 17) that provided multi-point optical interconnections between nodes. Each node can be routed optically to any other node by selecting a path through the switching fabric using a small number of intermediate hops. Arrays of binary optical routing switches have been made by integrating VCSELs with HBTs and photodetectors (PINs) in either a monolithic or hybrid format. Each node contains a pair of PIN/HBT/VCSEL switches, whose closely spaced PINs form a single optical input port, while their VCSELs provide two spatially separated optical output ports. An optical signal incident upon the PIN pair switches on one or both VCSELs

according to the routing control voltage applied to each switch. Each switch node can transmit or receive optical data, or to re-route it optically to other nodes.

We demonstrated the *reconfigurable, optically-cascaded, multi-stage switching operation of binary optical switch* arrays consisiting of PINs and HBTs integrated with VCSELs. The input nodes (pairs of PINs and HBTs) and output nodes (VCSELs) were monolithically integrated on two separate chips in order to individually optimize their characteristics and to achieve a large optical gain. When the binary optical switch can achieve a sufficient optical gain, the output of the first switch stage can be used to effect switching of the next stage, thus achieving optically cascaded switching operation. For the PIN/HBT/VCSEL switches usd in this demonstration, the dc current gain of the HBT is ~150, the external quantum efficiency of the PIN (including partition) is ~25%, and the external slope efficiency of the VCSEL is ~ 35%, giving an estimated optical gain of ~10-20.

Three linear binary optical switch arrays were used to demonstrate optically-cascaded switching operation (figure 17). The experimental configuration used to demonstrate optically-cascaded switching operation is shown in figure 18. An electrical input was applied to a node (figure 17a,b,c) in the first switch array to generate an optical output P_o, which is routed to another output port within the first array. The optical signal P_o then impinges on a switch node in 2, and produces a switched optical output P_1 with a net optical gain. By controlling the bias or routing control voltages, the switched signal P_1 can emerge as optical outputs from one or two VCSELs. This P_1 in turn impinges on another binary switch in stage 3 to produce optical output P_2 , again with an optical gain. Figures 17(d) and 17(e) show the electrical characteristics of the HBT and the optical characteristics of the VCSEL, respectively, while figure 17(f) shows the dc optical transfer characteristics of stage 2 (P_1 as a function of P_0) and stage 3 (P_2 as a function of P_1), respectively. Also shown are their derivatives, which represent the differential optical gain as a function of the input optical power for each stage. The optical gain of stage 2 has a peak value of ~18, while stage 3 has a peak value of ~4, which was due to variations in processing. The optical output power P_2 of the cascaded two-stage switching system, and the composite differential optical gain, dP_2/dP_o, are shown as a function of the input P_o in figure 17(f). The overall dc optical gain of the cascaded switches has a peak value of ~50.

The optical gain of these two stages of binary optical switches in cascaded operation have also been measured under ac modulation. At an input power level of P_1=20 μW and at a data rate of 50 Mb/s, the differential ac optical gain is dP_1/dP_o ~ 4 for the first stage, and dP_2/dP_1 ~2 for the second stage, giving an overall cascaded ac optical gain of dP_2/dP_o ~ 8.

2.3.h. Transceiver Characteristics of a PIN/HBT/VCSEL Switch and Transmission Characteristics through Optical fibers:

We have evaluated the transmission characteristics of VCSEL-based optical links, as well as the performance of the PIN/HBT/VCSEL routing switch as optical transceivers in fiber transmission experiments (fig. 19). For the former, high-performance VCSELs were directly modulated at a data rate of up to 1 Gb/s, using pseudorandom electrical data in a non-return-to-zero (NRZ) format, and the optical output is coupled into a single-mode or multi-mode silica fiber, respectively, with a coupling efficiency of >85% in each case. The transmission characteristics have been measured for fibers of varying lengths, ranging from 0.5 m to 1 km. A PIN photodiode and a transimpedance amplifier with a -3 dB bandwidth of 1.5 GHz was used

for the receiver. Pseudorandom optical data was successfully transmitted through 1 km of multi-mode fiber at a data rate of 1 Gb/s, with a bit-error-rate of better than 10^{-13}. However, in the single-mode case, evidence of dispersion can be seen after 1 km at 650 Mb/s, and more importantly, an error floor was observed below BER=10^{-10} as a result of mode-selective loss and the interference between coherent lasing modes.

The PIN/HBT/VCSEL switch was also used as both a transmitter and a receiver in optical transmission through optical fibers. Using switches that were used in the 500 Mb/s switching experiments, we modulated the switch at a data rate of between 650 Mb/s and 1 Gb/s, and transmitted the optical data through fibers with varying lengths, at the end of which it is detected by another switch and converted into electrical data. Again, single-mode transmssion experienced a BER floor caused by mode-selective loss, but multi-mode transmission was successfully demonstrated at 650 Mb/s across a 1 km span of fiber. The sensitivity of the switch as receiver is somewhat low (-14 dBm at 1 Gb/s) and BER=10^{-9}, and this is an area in which future switch designs must address. Different receiver circuits will be needed to improve the sensitivity of the receiver, and a different photodetector may also be needed to enhanced the responsivity of the detector (~50% quantum efficiency with 30% Fresnel loss). A future switch design will need to incorporate higher eelectronic gain, using multiple gain stages. For the very short distances that exist within a backplane environment, this may not be necessary, and improved component performance will likely suffice.

3. Future Prospects for this Technology:

In this program, we have successfully completed, indeed surpassed goals that we set out to achieve. We have defined and implemented a novel optical switching architecture, developed the integrated optoelectronics technology needed to implement it, and demonstrated the operation of a multi-stage optical switching network. We have thus fulfilled all of the milestones and more. However, our achievements to date are far from representative of the ultimate performance limit of this technology, which we have only begun to develop.

From the component viewpoint, we have only used 10% of the modulation bandwidth that the VCSEL (10 GHz), the PIN (>10 GHz) or the HBT (>50 GHz) is capable of, and the switching speed that can be achieved can be an order of magnitude higher (~5-10 Gb/s) than we have achieved. Nor have we fully exploited the very low switching energy that is available with a threshold switch with high optical gain. By pre-biasing each switch near threshold, and using switches with a higher differential optical gain (e.g., >20 per stage) switching can be achieved by very-low-energy optical input pulses and still provide sufficient optical gain and energy to be detected by the next switch stage. We have already demonstrated a switching energy in the 300 fJ range, and this can be significantly lowered. The sensitivity of the receiver can also be substantially increased, as we have mentioned above, so that a sensivitiy of <-25 dBm should be achievable at 1 Gb/s. An important criterion in any array performance is the density of power dissipation and thermal self-heating. The power dissipation of each switch stage can be reduced significantly (10x) from its present value (30 mW per switch, operating at 4V and 7.5 mA) to less than <2.5 mW per switch (2.5 V and 1 mA). This can be achieved by using low-threshold, oxide-confined VCSELs with submilliampere operating currents (e.g. 0.3 mA threshold, outputting 200 μW optical power at 1 mA, with a wall-plug efficiency of 20%). This can reduce the operating voltage of the switch to <2 V and its operating current to < 1 mA. A 16x16 array of switches each dissipating 2 mW will have a total dissipation of ~512 mW spread out across a 4 mm x 4 mm area (3 W/cm^2), which is quite manageable.

Perhaps the most promising potential for this technology will be achieved when it is combined with other multiplexing platforms, such as wavelength-division multiplexing (WDM). For example, if each element (or column in a 2D array)) of the switch array is assigned a different lasing wavelength, and selectively detects the same wavelength, then then all of the outputs can be wavelength-multiplexed together onto an optical fiber while keeping the SDM switching architecture intact and projecting it across much larger physical distances. For a 2D array, a linear fiber ribbon array will suffice to project these interconnections over LAN-like distances. The only technology modification needed would be a means of chirping the wavelengths of a VCSEL or photodetector array. A wavelength-selective photodetector array would enjoy the benefit of improved optical crosstalk suppression.

4. Smart Pixels as a Compact Optical Logic Processor: the Programmable Optical Logic Gate Array

In one view, smart pixels can be seen as parallel optical processing elements that perform a variety of functions on a two-dimensional array of input optical data to produce a logically and spatially modified, two-dimensional pattern of optical outputs. At one end, the smart pixel is a parallel optical link between intelligent electronic processing functions, where most if not all of the intelligence is vested in the electronic components. At the other extreme, the smart pixel can be an intelligent all-optical logic processor or computer. Individual smart pixel arrays can be monolithically integrated either as a space-invariant, single function logic array, or as a spatially inhomogeneous multi-functional optical logic circuit. Sequential smart pixel arrays can be optically cascaded to form a pipeline of distinct processing elements, or they can be configured as an optical programmable logic array (OPLA). These applications require a measure of optical gain and contrast, an optical fan-out of at least two, and reconfigurable optical interconnections.

Following our earlier demonstrations (1991-1992) of simple Boolean optical logic using latching PNPN/VCSEL logic gates and non-latching HPT/VCSEL logic gates, we proceeded to design programmable optical logic gates for a simpler and more functionally flexible optical logic architecture that can perform more complex logic functions using a minimum amount of optical and optoelectronic hardware. Programmable optical logic operations were demonstrated in 1993 using non-latching HPT/VCSEL binary optical switches without an electronic interface. Each array can be programmed at the gate level to perform different logic functions - AND and OR - by setting the threshold of each switch, which logically sums the input signals to produce a switched optical logic output, which can also be spatially routed to different output ports. The binary HPT/VCSEL optical switch was programmed to perform AND or OR logic with variable fan-out at a data rate of ~20 Mb/s. In order to execute arbitary logic sequences, several programmable arrays must be optically cascaded, and a multi-stage optical routing network is needed to reconfigure the optical routing paths between arrays. The complexity of the processor would thus rise exponentially with its functional complexity.

To alleviate this probelm, we designed an optical programmable logic gate array (OPLA), whose elements consisted of a monolithic array of binary PIN/HBT input nodes and a monolithic array of VCSEL output nodes, and an optically folded logic architecture that continuously re-uses a single OPLA. (figure 20) The complex logic functions are expressed in the sums of products form using dual-rail logic inputs and the AND and OR logic functions,

which are executed by optically cascading sequential logic gate arrays, each of which can be *programmed at the gate level* to perform *different logic operations* (AND or OR) *at selected nodes*, and to *spatially re-route* the optical logic outputs (with *optical gain* and a *selectable fan-out*) to provide the inputs for the next array, from one clock cycle to the next. Since each OPLA is reconfigurable, and the binary routing topolgy is fixed (shuffle network) from stage to stage, the same array can be re-used during each successive cycle, provided that the logic output of the previous cycle is optically buffered by a latching PNPN/VCSEL optical switch array. Thus a single OPLA and optical buffer can constitute the entire logic processor without further hardware, while the programming (control) voltages can be stored electronically as a reduced instruction set.

We have demonstrated programmable optical logic using the improved PIN/HBT/VCSEL switches, which provided a higher optical gain, a higher data rate (~100 Mb/s), and both electrical and optical logic inputs or outputs. Programmable optical logic was demonstrated using either electrical or optical inputs at 100 Mb/s, and more complex logic functions were achieved by cascading two OPLAs. Figures 20a shows the design of an OPLA containing an array of binary PIN/HBT/VCSEL switch nodes, and 20b shows the experimental arrangement that is used to demonstrate cascaded, multi-stage optical logic operation. An optical (A_{opt}) or electrical (A_{el}) logic input is applied to each input node through the PIN-pair or through the base terminal of the HBT, respectively. This produces amplified currents that modulate the optical output P_{out} of a VCSEL, which is pre-biased below threshold. Depending on the bias and routing control voltages, V_{c1} and V_{c2}, the inputs are spatially routed to one or more VCSEL output ports. The input signals from two different input nodes (e.g., A_{opt} and B_{opt}) can be routed to a single VCSEL output port to be logically summed. Since the VCSEL is a threshold device, these sums can determine the logic outcome, e.g., either (A-OR-B) or (A-AND B) logic operation can be executed, depending on the dc prebias level of each VCSEL. The in-plane pairing of nodes (e.g., shuffle connections) defines the range of possible spatial routing configurations within a single stage, and complete routing of the optical logic signals is accomplished using successive stages, which collectively define a logic operation sequence.

The logic operation of the first OPLA at 100 Mb/s is shown in figures 20c and 20d, using either optical or electrical logic inputs, respectively. The optical logic inputs A and B are applied to the PINs at two different input ports, while the *electrical logic inputs* C and D are applied to the base terminal of each HBT. These inputs produce amplified currents that are routed to and summed at a single VCSEL output port, producing optical logic output (A-OR-B) or (A-AND-B), depedning on the VCSEL pre-bias level. The rise and fall times are ~5 ns, and the switching energy is ~300 fJ.

Figure 21 summarizes the results of a cascaded optical logic sequence, stage-by-stage, starting with the optical logic inputs A and B and electrical inputs C and D. The optical outputs (*e.g.*, A+B and C•D) of the VCSELs in the first logic array provide the inputs for the nodes of the next array. Since each array is programmable at the individual gate level, different cascaded logic operations can be performed in parallel by setting the appropriate control voltages. The optical logic outputs of the first stage - (A+B), (C+D) and (C•D) - are routed to the appropriate nodes in the second array, where they are logically summed. The latter array then performs AND or OR logic on these inputs to produce the optical logic outputs [(A+B)+(C•D)], or [(A+B)•(C•D)], respectively. This demonstration of cascaded optical logic illustrates the flexibility afforded by programmability of the switch arrays. Much greater flexibility can be

achieved by replacing the non-latching HPT/VCSEL switches with latching PNPN/VCSEL switches. This allows a single programmable logic array to be continuously reconfigured and re-used for each successive logic operation, while an optical buffer memory stores the outputs of the previous stage to provide inputs for the next stage. Arbitrary logic functions can thus be performed using a simple 2-chip architecture. This was not demonstrated, however, because of the lack of resource to mount a serious packaging effort.

Finally, fig. 22 illustrates the concept of reconfiguring a single programmable optical logic gate array to perform different sequential optical logic and routing operations, while buffering the output of each stage in an array of latching PNPN/VCSEL optical memory switches. The specific function of of a binary addition is used to demonstrate this concept.

5. Figure Captions:

Figure 1. (a) The proton-implant-isolated structure, (b) electrical characteristics, and (c) lasing characteristics of a typical 16 μm diameter VCSEL with continuous, bi-parabolically-graded DBR mirror heterointerfaces grown by MOCVD. Low operating voltages and high power conversion efficiency are achieved.

Figure 2. The characteristics and SEM cross section of an oxide-confined VCSEL with a ~4 μm active area.

Figure 3. The optical transmission characteristics of a VCSEL based optical link using (a) different lengths of a single mode optical fiber at 650 Mb/s, and (b) a 1 km length of graded-index multi-mode fiber at 1 Gb/s.

Figure 4. Several configuration of a monolithic HPT/VCSEL optical switch. The common emitter switch configuration requires a common p-substrate, while the emitter follower configuration requires a common n-substrate. Also shown are the electrical and lasing characteristics of VCSELs grown on a p-substrate and on an n-substrate.

Figure 5. A generic parallel optical array processor using 2D arrays of VCSELs and other VCSEL-based switches, detectors, and logic gates, which can perform a variety of different functions, including switching, logic, routing, and memory.

Figure 6. A reconfigurable, board-to-board, multi-stage optical interconnection network. Each board contains a number of processors with parallel access to a parallel optical data bus, whose traffic is regulated by a two-dimensional array of optical switches on each board, each of which can communicate directly with an electronic processor on that board. Also shown are a three-stage routing network and a photograph of one of the monolithic switching arrays.

Figure 7. A reconfigurable, closed-ring, optical interconnect architecture linking clusters of nodes through parallel optical paths set by optoelectronic switch arrays, which contain electrical input and output ports. Each switch contains a segmented HPT interconnected individually to different VCSELs in the array, and can be programmed to receive, transmit, or re-route optical signals. Schematic layout of a two-stage optical backplane interconnecting 4 electronic processors (2 per stage). Each processor contains an optoelectronic interface to the switch, through which it can transmit or receive optical data, as well as to bypass the incoming optical data or to re-route it to another stage.

Figure 8. The optical switching characteristics (above) and electrical characteristics (below) of the three types of optical switches that are described in figure 7, which have (a) non-latching, (b) bistable, and (c) latching characteristics, respectively.

Figure 9. The epilayer structure, photomicrograph, and circuit design of monolithic, (a) 2x2 and (b) 1x2, binary optical routing switches with optical fan-out. The 2x2 switch is a combination of two 1x2 switches. Also shown schematically are the modes of operation for each switch, including routing, fan-out, bypass and exchange.

Fig. 10. (a) The routing functions and photomicrograph of a reconfigurable 1x2 binary HPT/VCSEL optical switch, which can be dynamically reconfigured to route input optical data to different optical output ports with fan-out. (b) Experimental demonstration of 1x2 optical switching, showing the routing control voltages and the optical output channels for the cases of (a) no fan-out, and (b) an optical fan-out of 2.

Fig. 11. (a) The routing functions and photomicrograph of a reconfigurable 2x2 binary HPT/VCSEL optical switch, which can be dynamically reconfigured to perform optical bypass and exchange routing operations. (b) Experimental demonstration of 2x2 optical switching, showing the control voltages, the input and output optical channels, and the bypass and exchange operations.

Fig. 12. A linear array of reconfigurable binary HPT/VCSEL switches, which can be programmed to perform different optical logic and spatial routing functions with variable optical fan-out by setting the control voltages of each switch (as shown). Each node contains a two-segment HPT, whose segments are connected to different VCSELs in a shuffle network geometry. Different arrays of switches with the same routing geometry can be optically cascaded to perform more complex functions.

Figure 13. The dc characteristics of a monolithic HBT/VCSEL switch, showing (a) its common-emitter characteristics, (b) VCSEL optical output vs switch bias voltage, (c) current gain vs collector current, and (d) the electrical to optical power conversion.

Figure 14. (Below) The epilayer design and device layout of a monolithic optoelectronic switch integrating a VCSEL with a HBT, which provides a rudimentary optoelectronic interface between the optical switching fabric and an electronic processor, which modulates the VCSEL to produce an optical output. Also shown (above) are the electrical and optical characteristics of the switch and its electrical-to-optical conversion efficiency.

Figure 14. (a) Functions of a monolithic three-terminal HPT/VCSEL switch, (b) the small-signal response of the HPT and the switch, and (c) its large-signal optical modulation response at 500 Mb/s.

Figure 15. (a) Photomicrograph, and (b) epilayer structure of a monolithic HPT/VCSEL switch. (c) Schematic diagram of the emitter-follow circuit, with optical input P_{in}, electrical input E_{in}, optical output P_{out}, and electrical output I_{out}, (d) Time traces showing the electrical (trace 3) and optical (trace 4) output of the switch in response to the combined electrical (trace 1) and optical (trace 2) input data at 200 Mb/s. Each output contains replicas of both inputs. (e) Eye-diagrams showing the optical (lower traces) and electrical (upper traces) response of the switch to large-signal,

pseudorandom modulation by optical (left) and electrical (right) input data at 200 Mb/s.

Figure 16. (a) The circuit design, (b) epilayer structure, and (c) photomicrograph of a binary PIN/HBT/VCSEL routing switch containing a segmented PIN input port and two VCSEL output ports. The lower traces show the optical output of the switch in response to (d) electrical, and (e) optical input modulation at a data rate of 400 Mb/s, while (f) shows the optical output from VCSEL A and VCSEL B of the binary optical switch in response to optical input modulation at 500 Mb/s, showing that the switched output emerges alternately from output channel A or output channel B as the routing control voltage is toggled between the two individual switches.

Figure 17. (a) The circuit design, (b) layout of a reconfigurable binary PIN/HBT/VCSEL optical routing switch. (c) Optically-cascaded, multi-stage switching network using arrays of binary switches to perofrm optical routing and optoelectronic conversion functions. (e) shows the common-emitter characteristics of the switch, (e) shows the lasing and electrical characteristics of the VCSEL, and (f) shows the differential optical gain of each of the two stages under optically cascaded dc switching operations.

Figure 18. The experimental setup used to demonstrate optically-cascaded, multi-stage switching operation.

Figure 19. (a) The experimental configuration for studying optical transmission through an optical fiber, using two PIN/HBT/VCSEL switches as the optical transmitter and optical receiver, respectively. (b) The bit error rate as a function of received optical power, for single-mode (SM) fiber transmission at 650 Mb/s, and multi-mode (MM) fiber transmission at 1 Gb/s.

Figure 20. (a) The circuit design of a programmable logic gate (inset), and the experimental arrangement used to demonstrate optically cascaded logic operation using two programmable optical gate arrays. Optical logic functions - AND and OR - are performed using (b) electrical, and (c) optical logic inputs and a programmable optical logic gate array. The maximum data rate here is 100 Mb/s.

Figure 21. Two-stage, cascaded optical logic functions on four logic inputs - electrical inputs A and B, and optical inputs C and D. The first stage produces logic outputs: (a) (A+B) and (C•D), and (b) (A+B) and (C+D). The second stage operates on the logic outputs of the first stage, fans-out the logic signals, and performs the logic functions - OR and AND - on these cascaded logic inputs.

Figure 22. A schematic representation of the design of a programmable optical logic gate array consisting of integrated arrays of optically cascadable binary PIN/HBT/VCSEL switches, whose functions (logic, routing, fanout) can be programmed at the individual gate level. A logic processing sequence can be executed with an optically-folded architecture, using only a single programmable logic gate array that is reconfigured and re-used from one cycle to the next, while the optical outputs of the previous cycle are stored in a latching optical buffer memory.

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ABSTRACT

This program began with the objective of developing a novel optical interconnect technology that would provide parallel optical interconnections between electronic processing elements in a dynamically reconfigurable manner. The goal was to develop a switching fabric consisting of integrated optoelectronic switch arrays that offer a very compact, very-high-information-throughput, optical interconnect architecture. The technology that we had chosen was based on the monolithic integration of vertical-cavity surface-emitting lasers (VCSELs) with other photonic and electronic technologies, including heterojunction photo-transistors (HPTs) and photothyristors (PNPNs), PIN and MSM photodiodes, and heterojunction bipolar transistors (HBTs). We have played a leading role in the development of monolithic optoelectronic integrated circuit (OEIC) technology based on VCSELs, as well as advancing the state-of-the-art in VCSEL technology itself.

The integration of VCSELs with other photonic and electronic components has produced novel optical and optoelectronic devices with a host of potential applications. Combining VCSELs with heterojunction phototransistors (HPTs) and photothyristors produced several families of high performance optical switches with alternatively latching, non-latching, or bistable switching characteristics, and with varying degrees of optical gain and contrast. Non-latching optical switches integrating VCSELs and HPTs are particularly useful for optical switching and spatial routing operations.

We have developed an optical interconnect architecture and a high-speed OEIC switching technology that can provide reconfigurable interconnections between electronic processors, allowing them to communicate through a network of integrated optoelectronic transceivers and compact, monolithic, space-division-multiplexed switches that provide an optical link to other nodes and electrical access to each processor. These reconfigurable binary HPT/VCSEL switches can detect, regenerate, and spatially re-route optical data, and can be programmed by simple voltages to perform different optical routing, fan-out, and logic functions. Arrays of switches with high optical gain were optically cascaded to form a multi-stage optical switching network that provide multi-point interconnections between nodes, through which multiple data channels can be routed in parallel without intermediate optoelectronic signal conversion. The functional capabilities of this reconfigurable optical switching fabric have been demonstrated at a data rate of >500 Mb/s.

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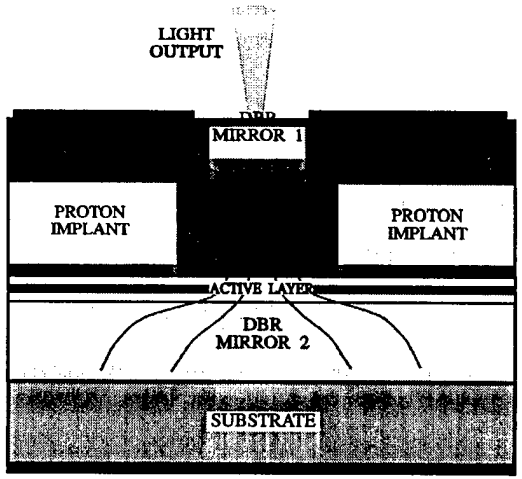
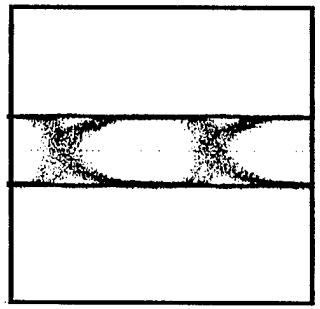
HIGH PERFORMANCE VCSELS FOR OPTICAL INTERCONNECTS

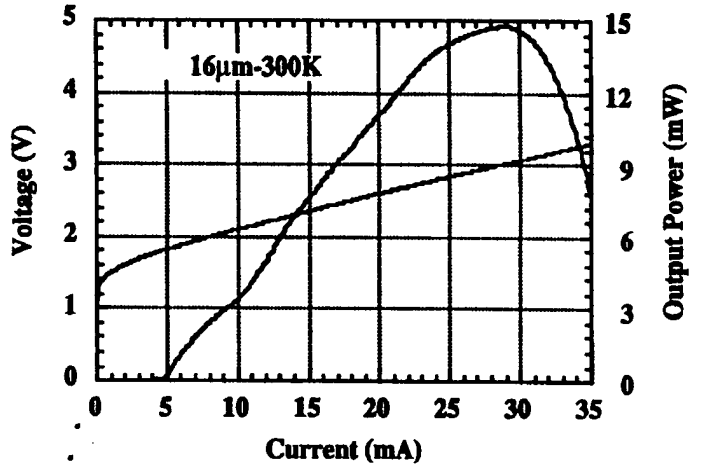
PROTON-IMPLANT-ISOLATED VCSEL

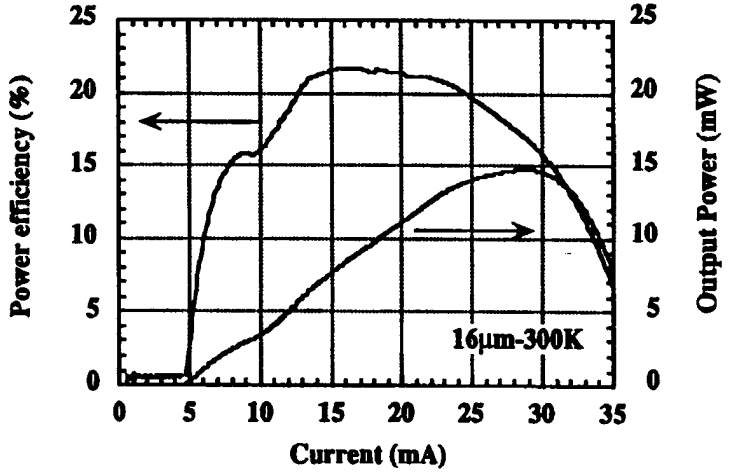




200 ps/div.

1 Gb/s, (2^{23}-1) NRZ, PRBS Data Transmission through 1km of Multi-Mode Fiber
Bit Error Rate < 1E-13





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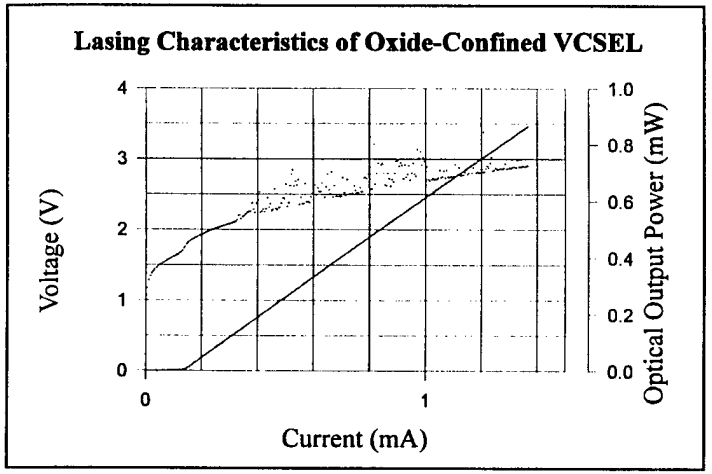
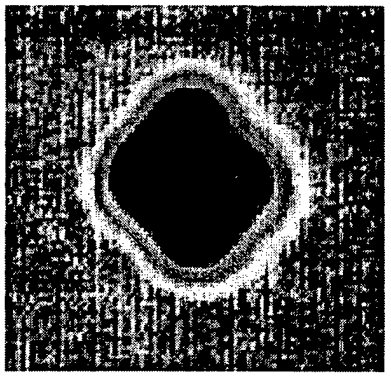
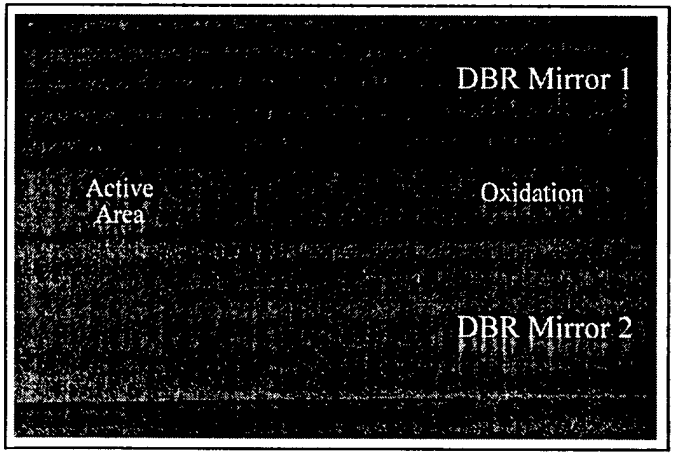
LOW-THRESHOLD OXIDE-CONFINED VERTICAL-CAVITY SURFACE-EMITTING LASER



Single Transverse Mode VCSEL



SEM Cross-Section of Oxidized VCSEL



Oxidized VCSEL

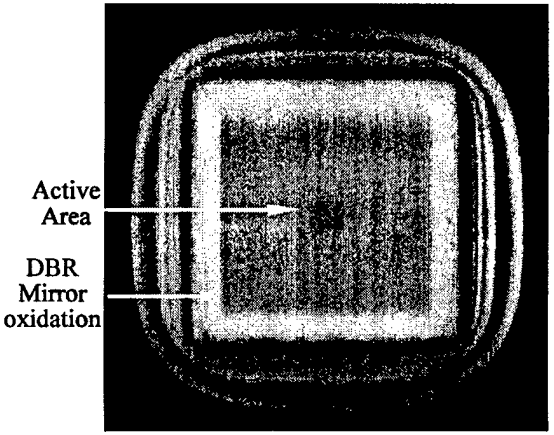
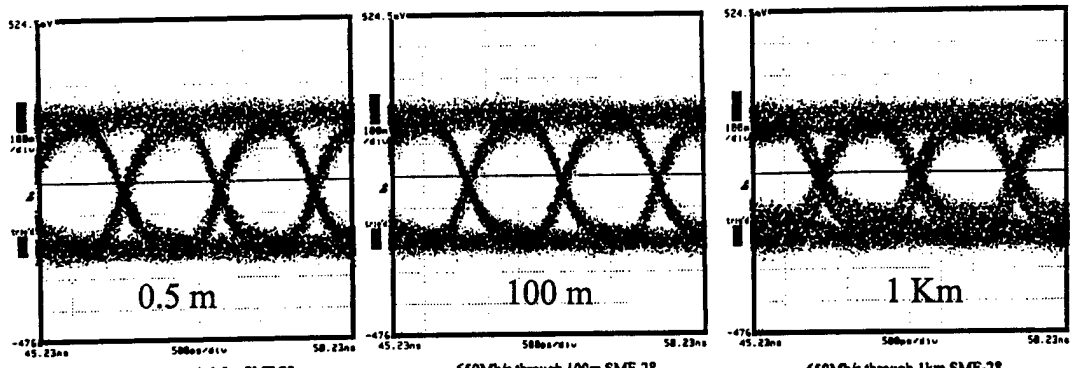


FIG. 2

(a) 650 MB/S TRANSMISSION OF 850 NM VCSEL THROUGH A SINGLE-MODE FIBER

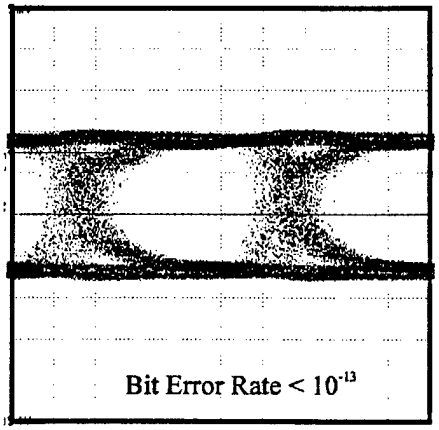


650Mb/s through 0.5m SMF-28
BER<5E-10

650Mb/s through 100m SMF-28
BER<5E-10

650Mb/s through 1km SMF-28
BER<7E-10

(b) 1 Gb/s NRZ Transmission through 1km of Multi-Mode Fiber



200 ps/div.

FIG. 3

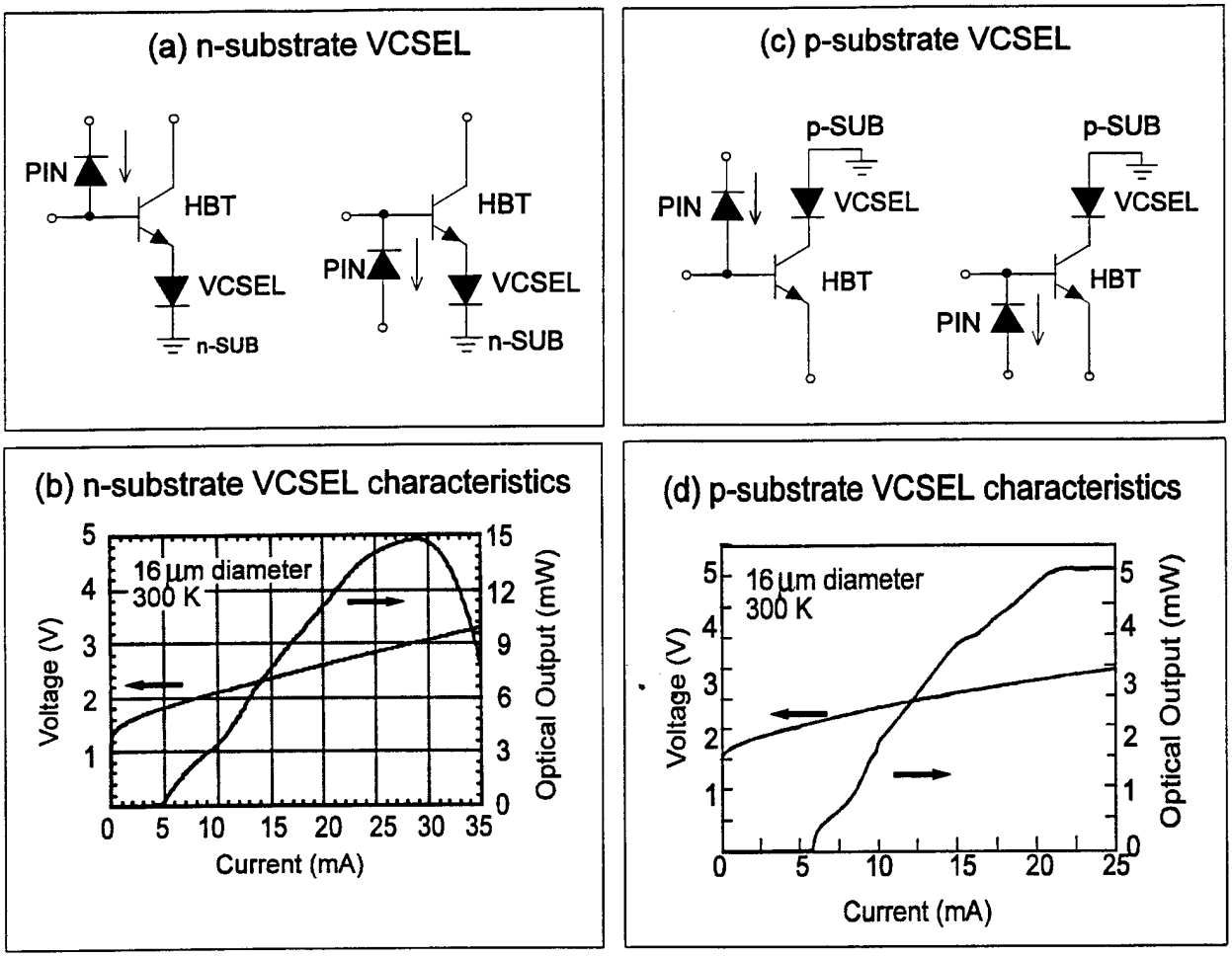

(a) n-substrate VCSEL
PIN
HBT
VCSEL
n-SUB
PIN
HBT
VCSEL
n-SUB
(c) p-substrate VCSEL
p-SUB
PIN
VCSEL
HBT
p-SUB
VCSEL
HBT
PIN
(b) n-substrate VCSEL characteristics
16 µm diameter
300 K
Voltage (V)
Optical Output (mW)
Current (mA)
0 5 10 15 20 25 30 35
1 2 3 4 5
0 3 6 9 12 15
(d) p-substrate VCSEL characteristics
16 µm diameter
300 K
Voltage (V)
Optical Output (mW)
Current (mA)
0 5 10 15 20 25
1 2 3 4 5
0 1 2 3 4 5

Figure (4).

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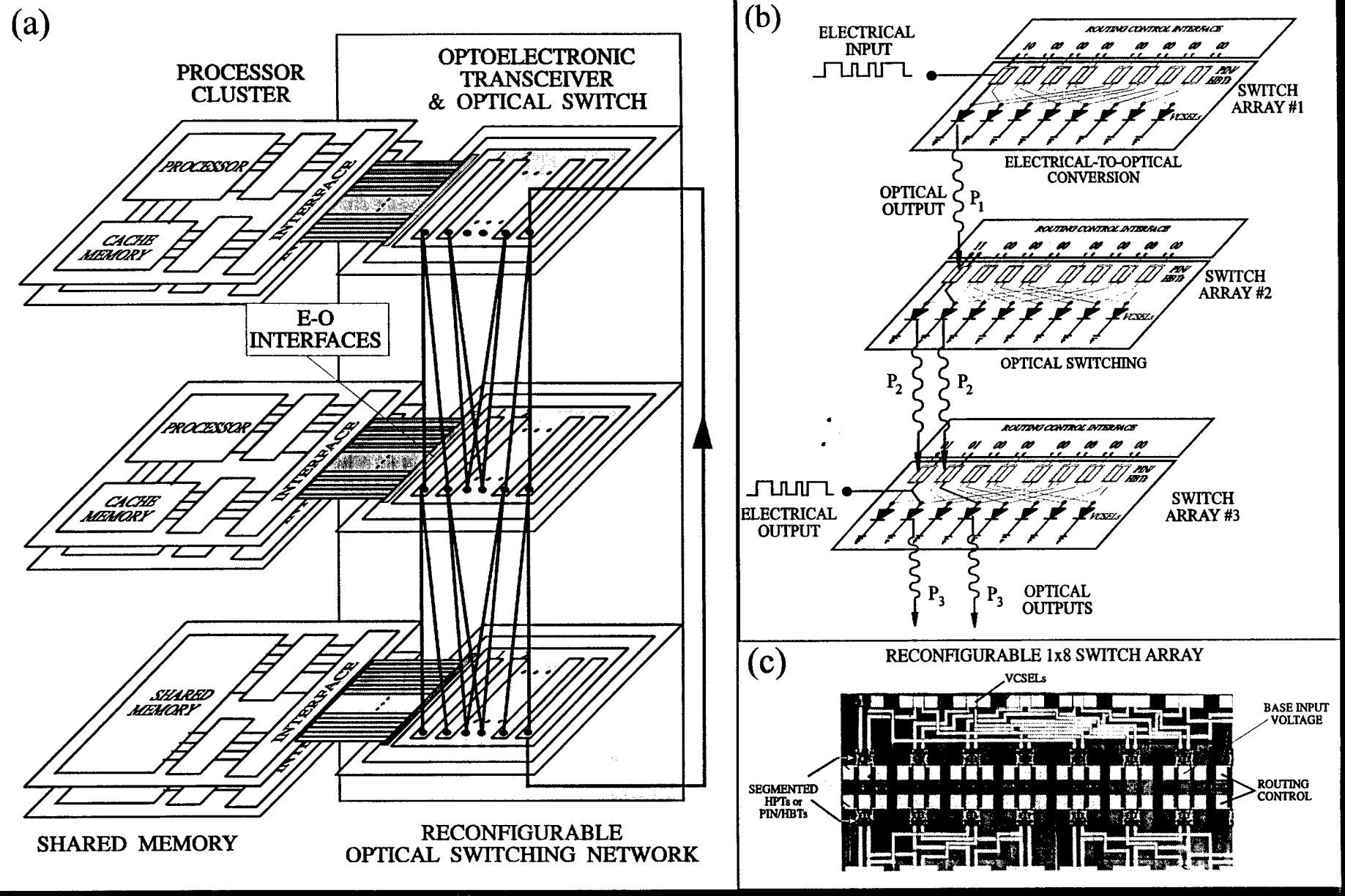
Fig. 5



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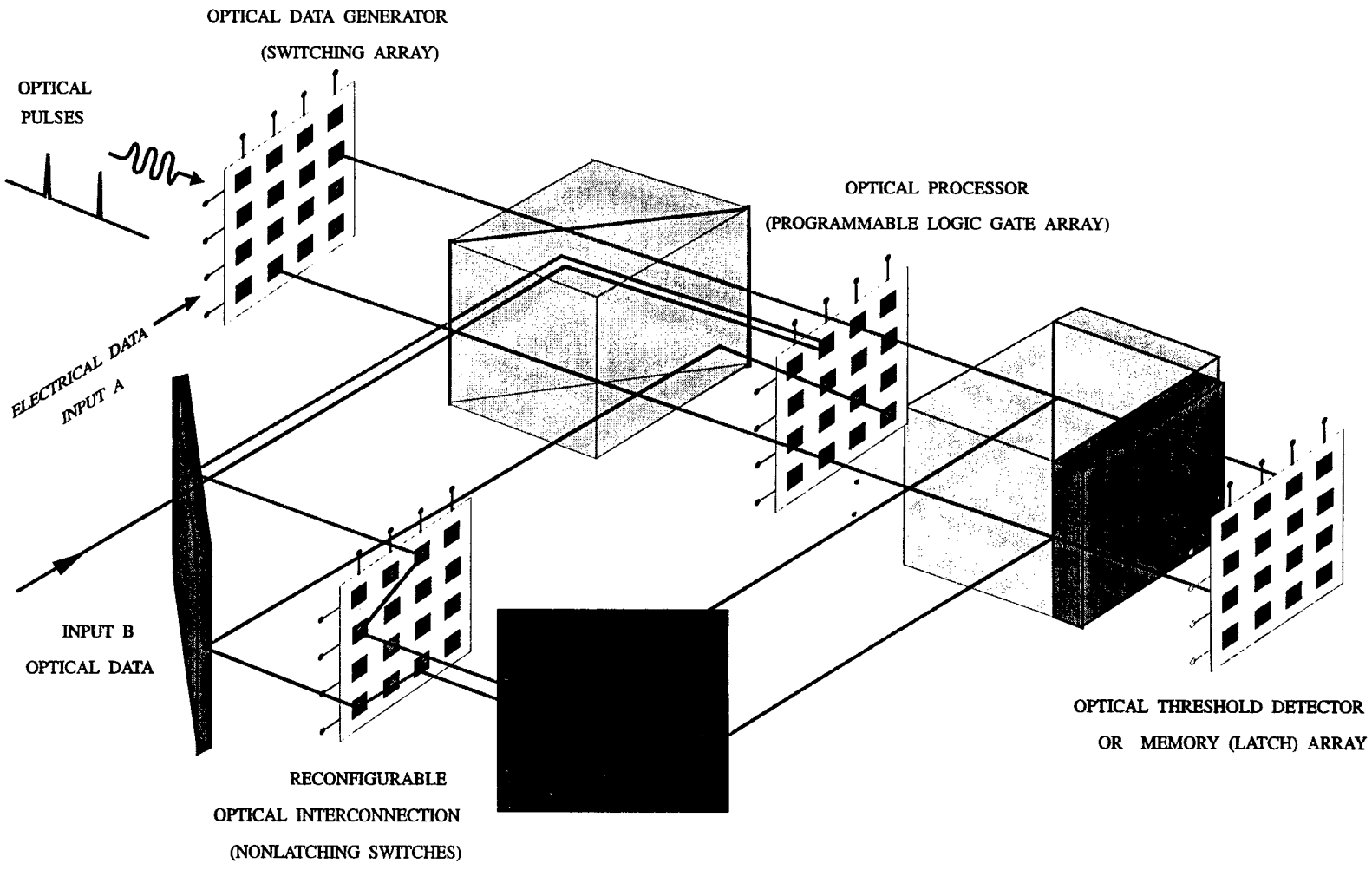

Fig. 9

PARALLEL OPTICAL ARRAY PROCESSOR

INTEGRATED VCSEL/PHOTOTHYRISTOR AND VCSEL/PHOTOTRANSISTOR OPTICAL SWITCHES

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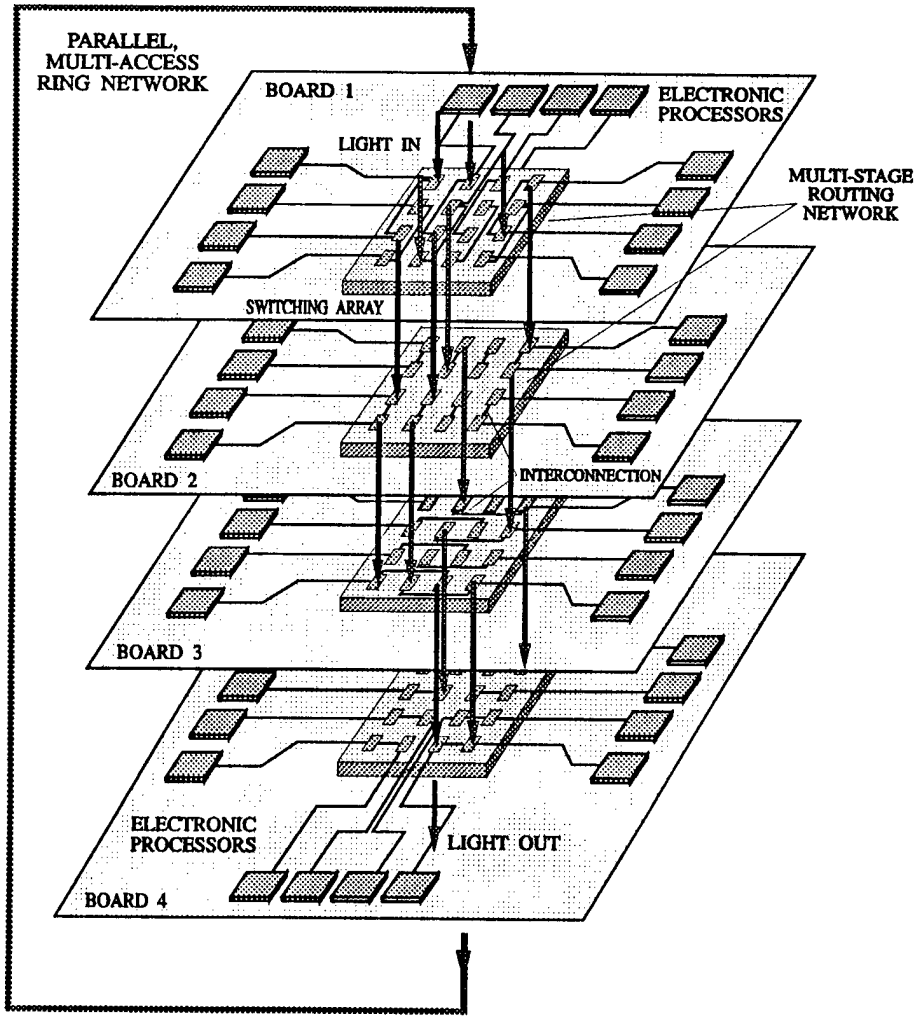
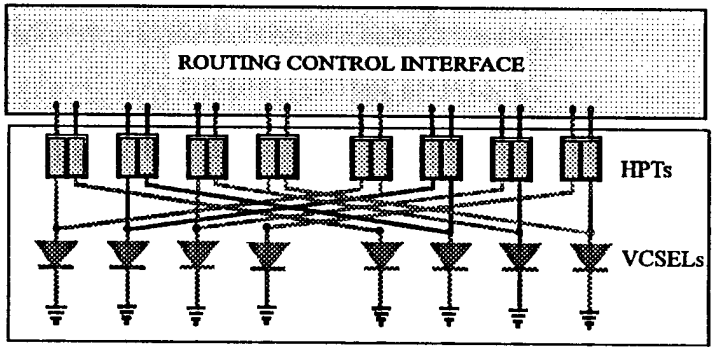
TWO-DIMENSIONAL, RECONFIGURABLE INTER-BOARD OPTICAL INTERCONNECT



MONOLITHIC OPTOELECTRONIC SWITCHING FABRIC



INTERPROCESSOR OPTICAL INTERCONNECT

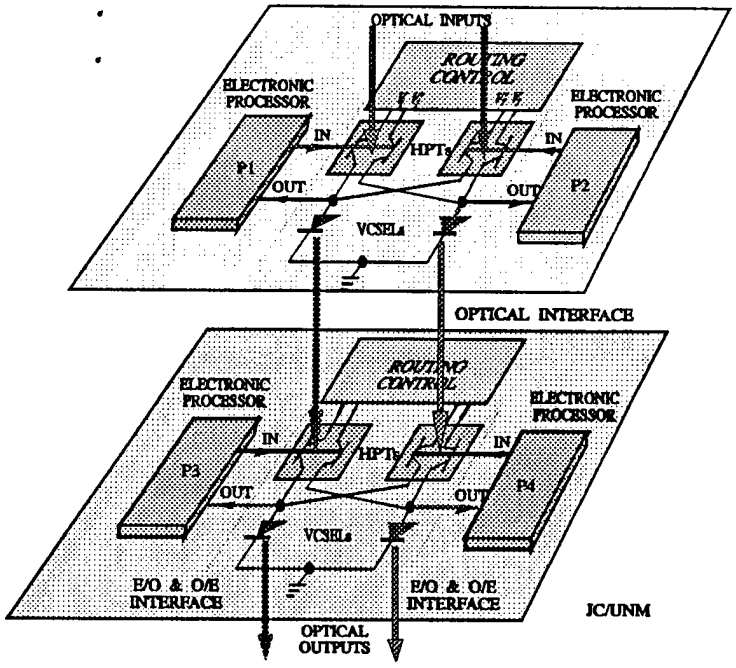


Fig. 7

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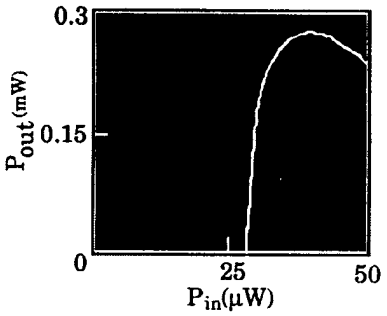
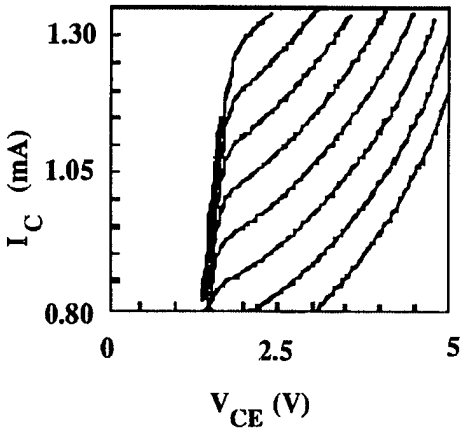
MULTI-FUNCTIONAL PHOTONIC SWITCHES

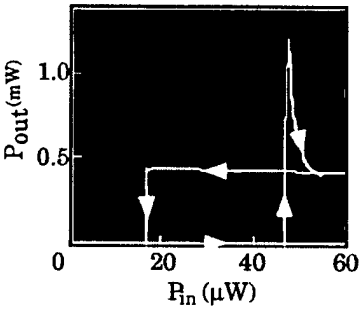


NON-LATCHING

VCSEL/PHOTOTRANSISTOR SWITCH

NO POSITIVE FEEDBACK

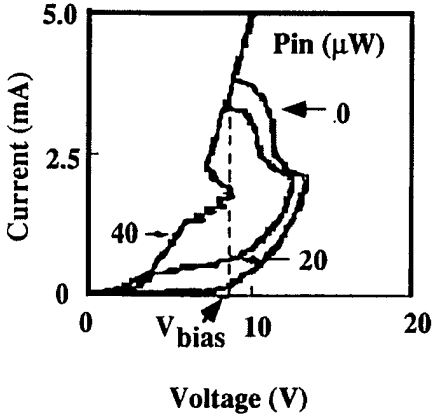


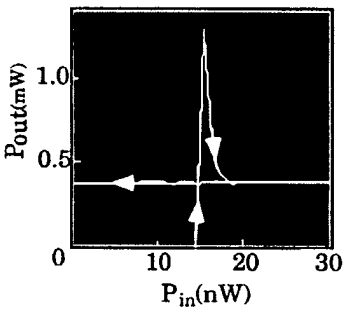


BISTABLE

VCSEL/PHOTOTHYRISTOR SWITCH

WEAK POSITIVE FEEDBACK

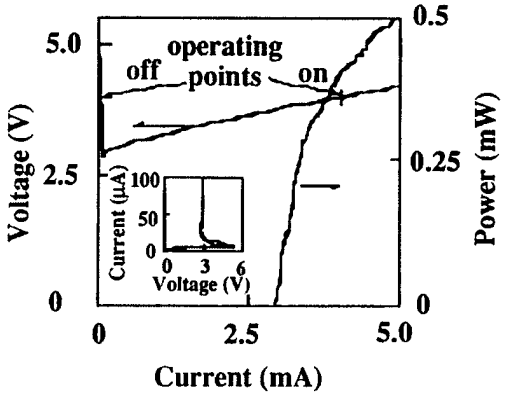




LATCHING

VCSEL/PHOTOTHYRISTOR SWITCH

STRONG POSITIVE FEEDBACK



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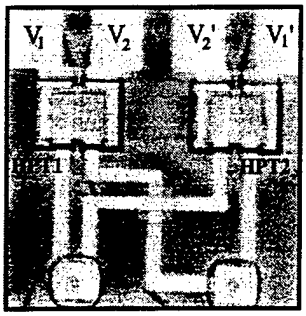
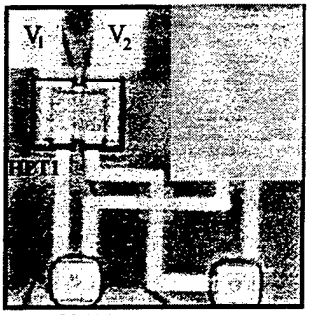
BINARY SWITCH LAYOUT

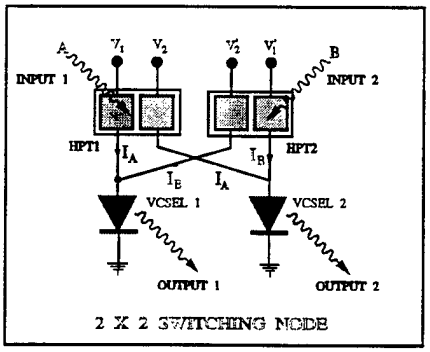


VCSEL1 VCSEL2

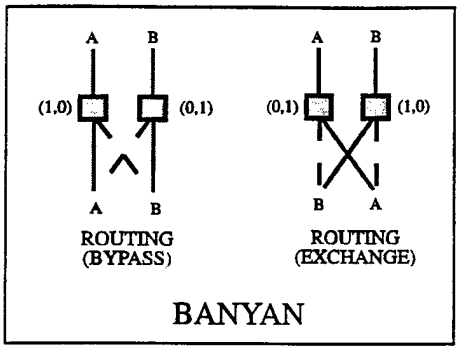


VCSEL1 VCSEL2

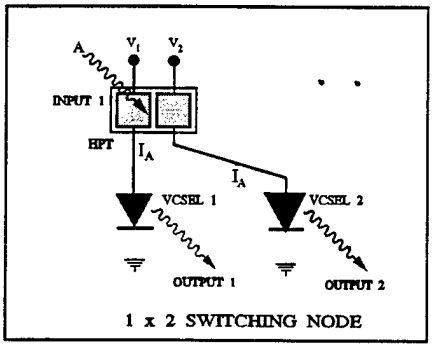
RECONFIGURABLE HPT/VCSEL OPTICAL SWITCHES



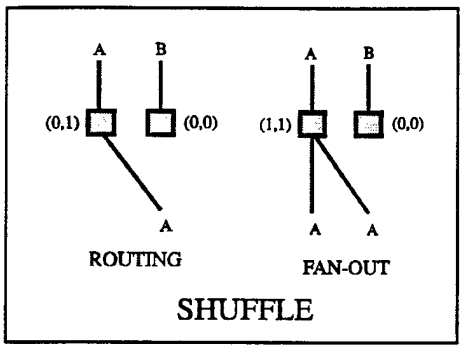
2 X 2 SWITCHING NODE



BANYAN



1 x 2 SWITCHING NODE



SHUFFLE

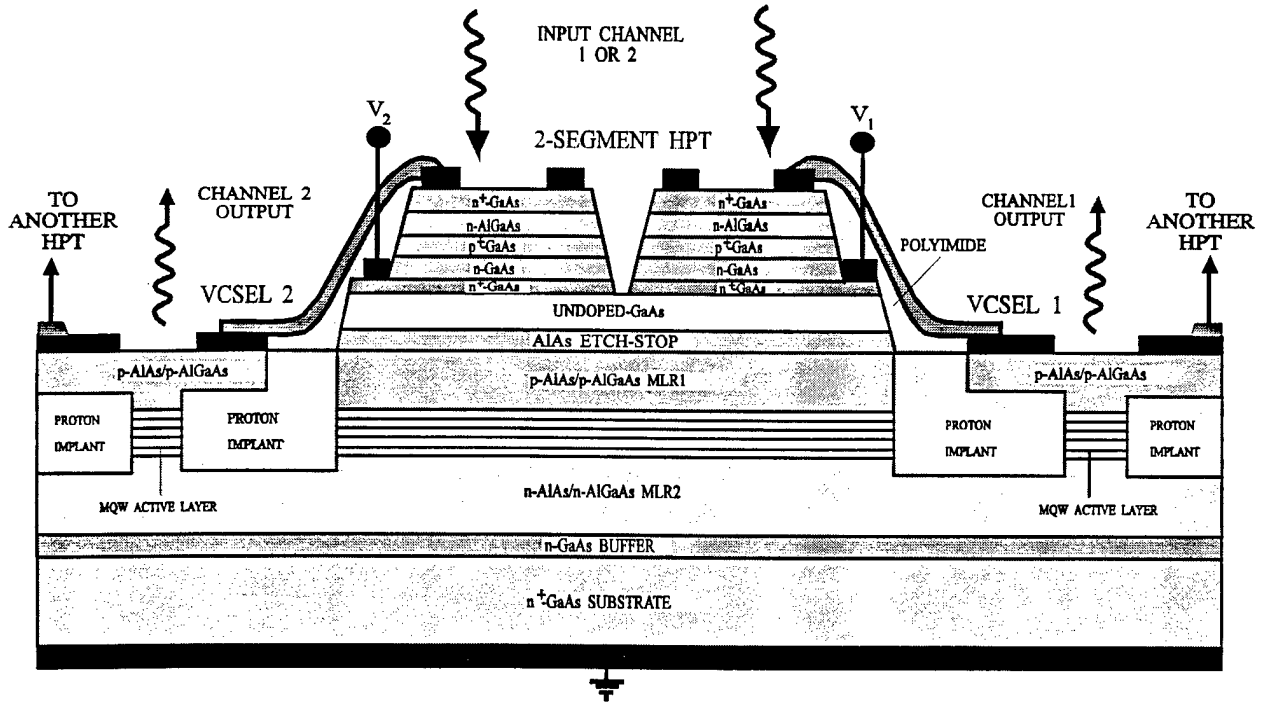


FIG. 9

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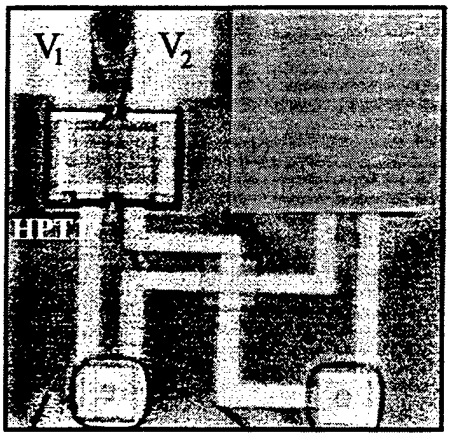
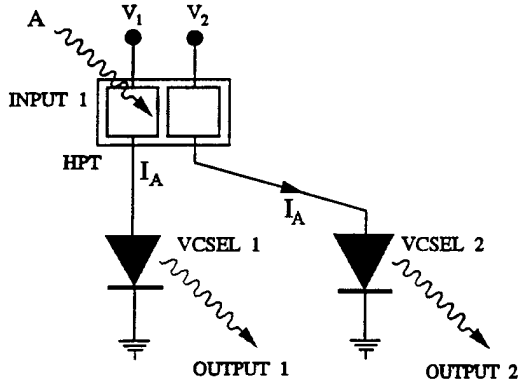
RECONFIGURABLE, MONOLITHIC HPT/VCSEL BINARY OPTICAL ROUTING SWITCH WITH FAN-OUT

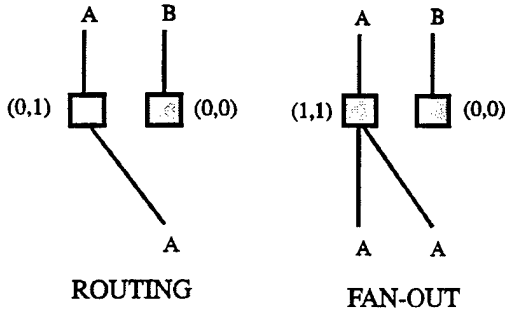
1x2 BINARY ROUTING SWITCH



VCSEL1 VCSEL2



1 x 2 SWITCHING NODE



OPTICAL ROUTING AND FAN-OUT

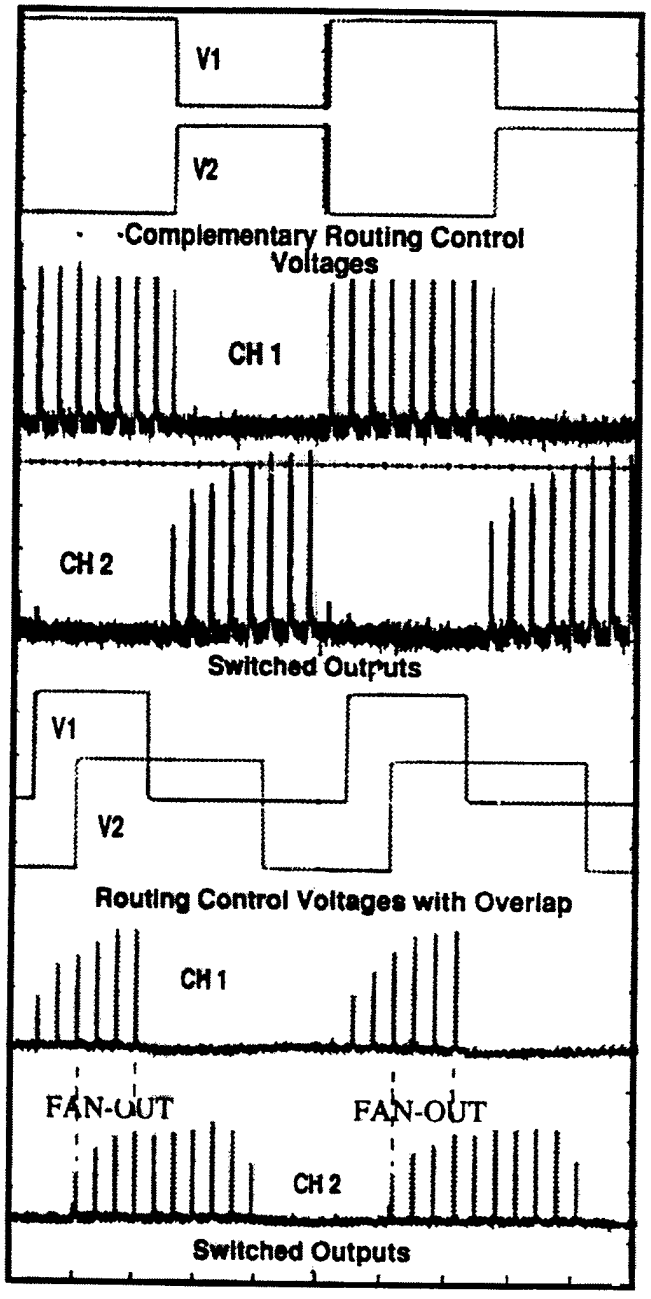


FIG. 10

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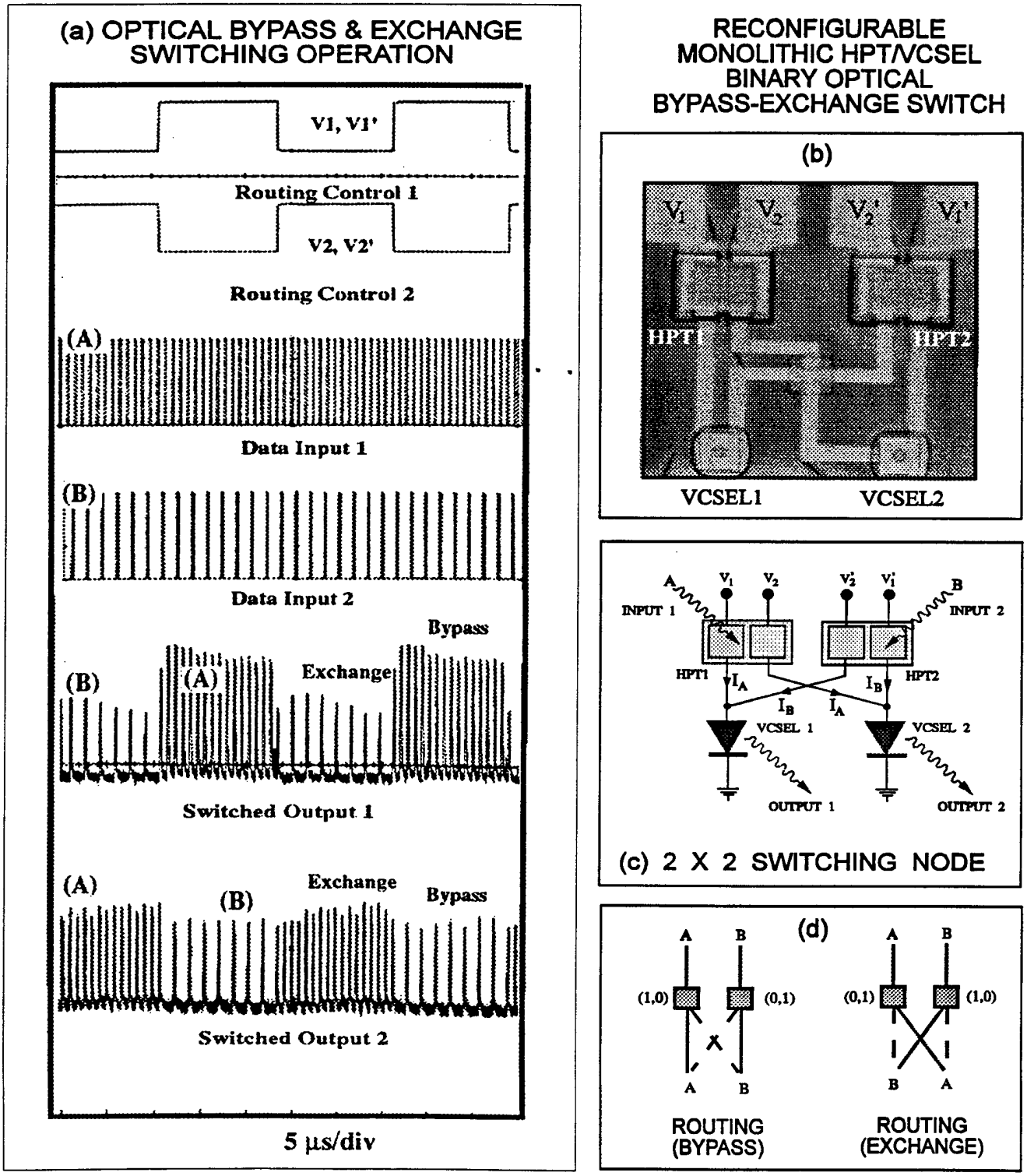

Figure . (a) Optical bypass-exchange routing operation using a reconfigurable binary optical routing switch consisting of two pairs of monolithic HPT/VCSEL switches. The switch layout is shown in (b), its circuit diagram in (c), and its switching functions in (d).

FIG. 11

PROGRAMMABLE OPTICAL SWITCH ARRAY FUNCTIONS

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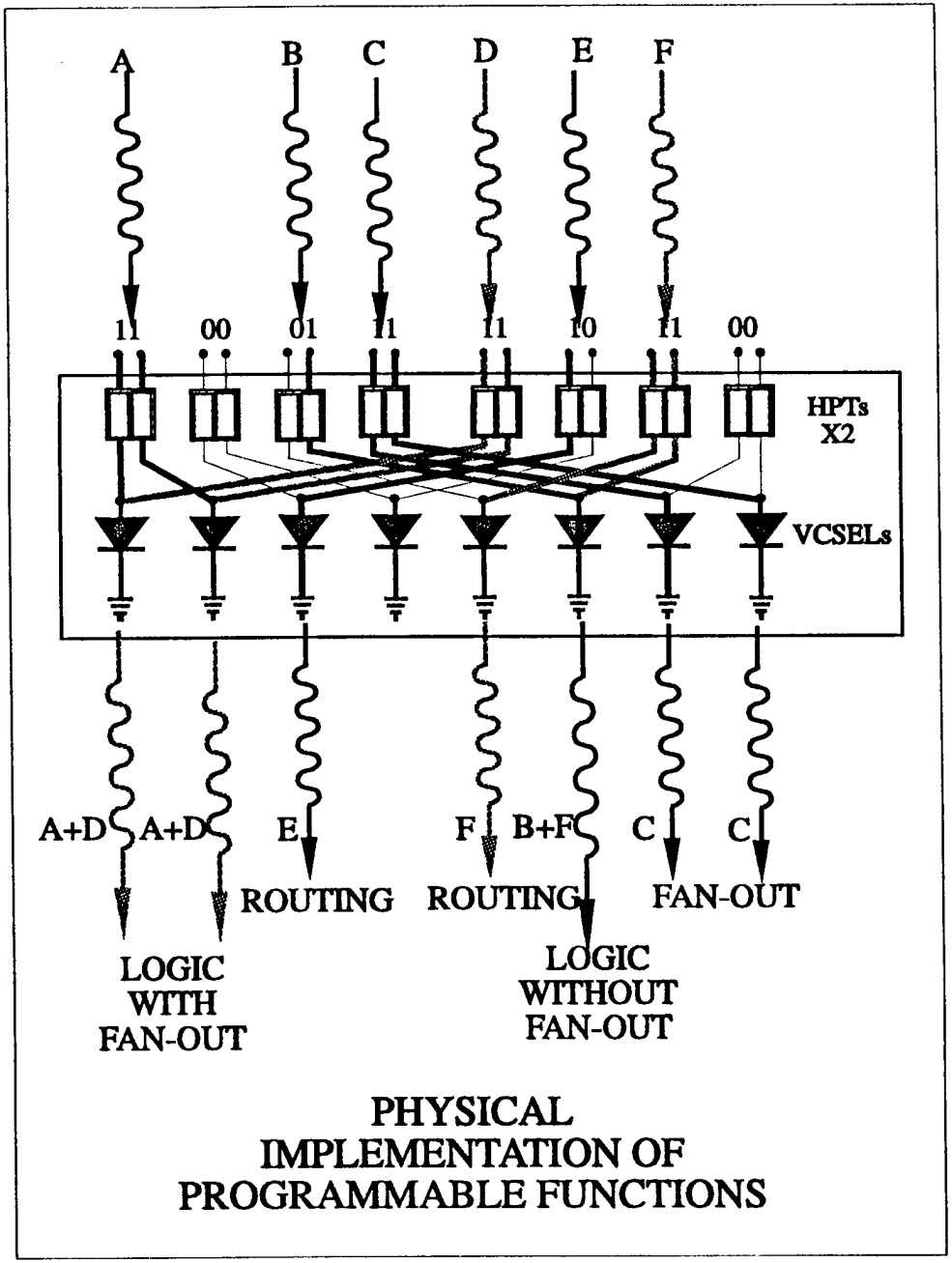
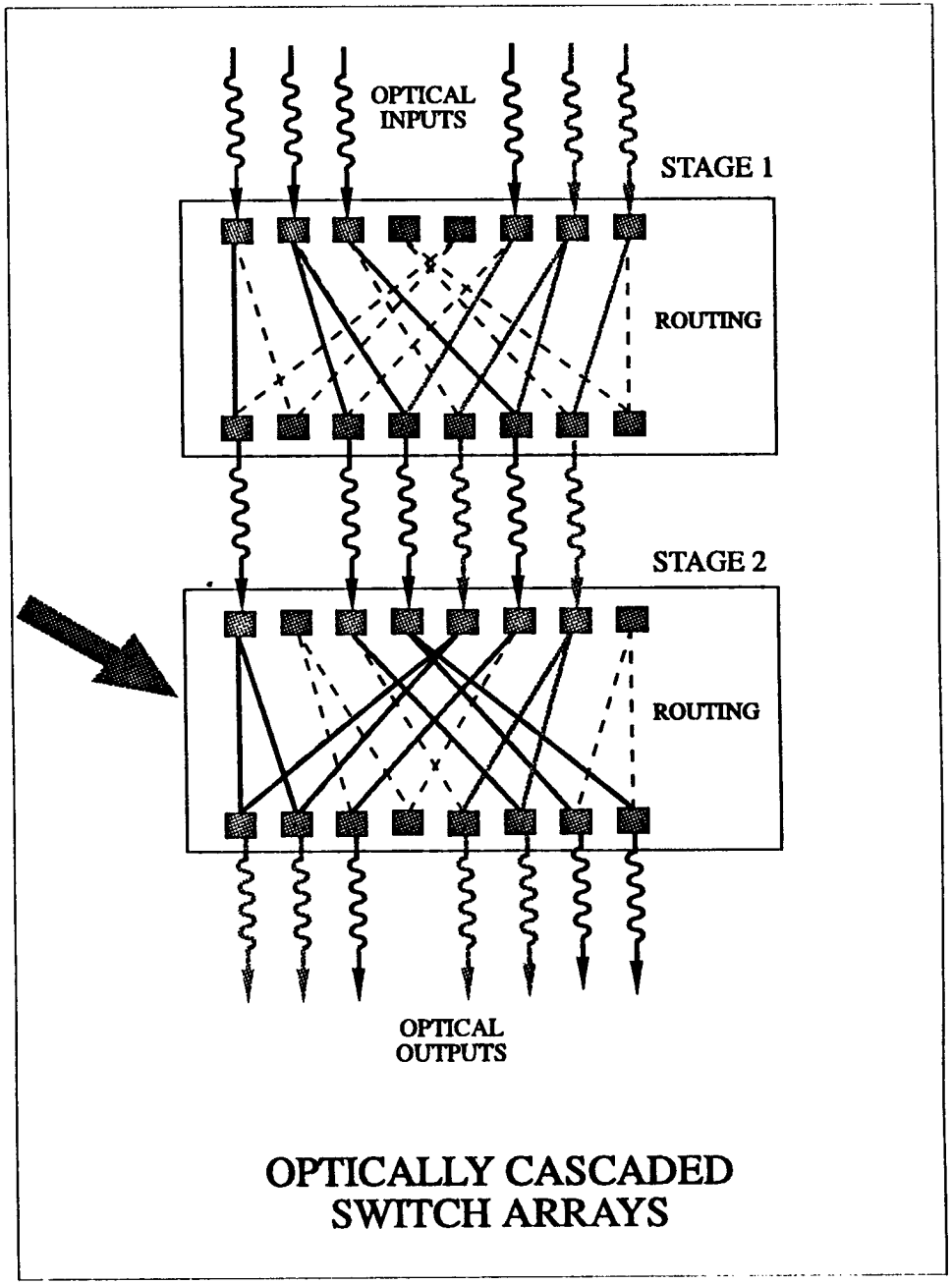


PHYSICAL IMPLEMENTATION OF PROGRAMMABLE FUNCTIONS



OPTICALLY CASCADED SWITCH ARRAYS

Fig. 12

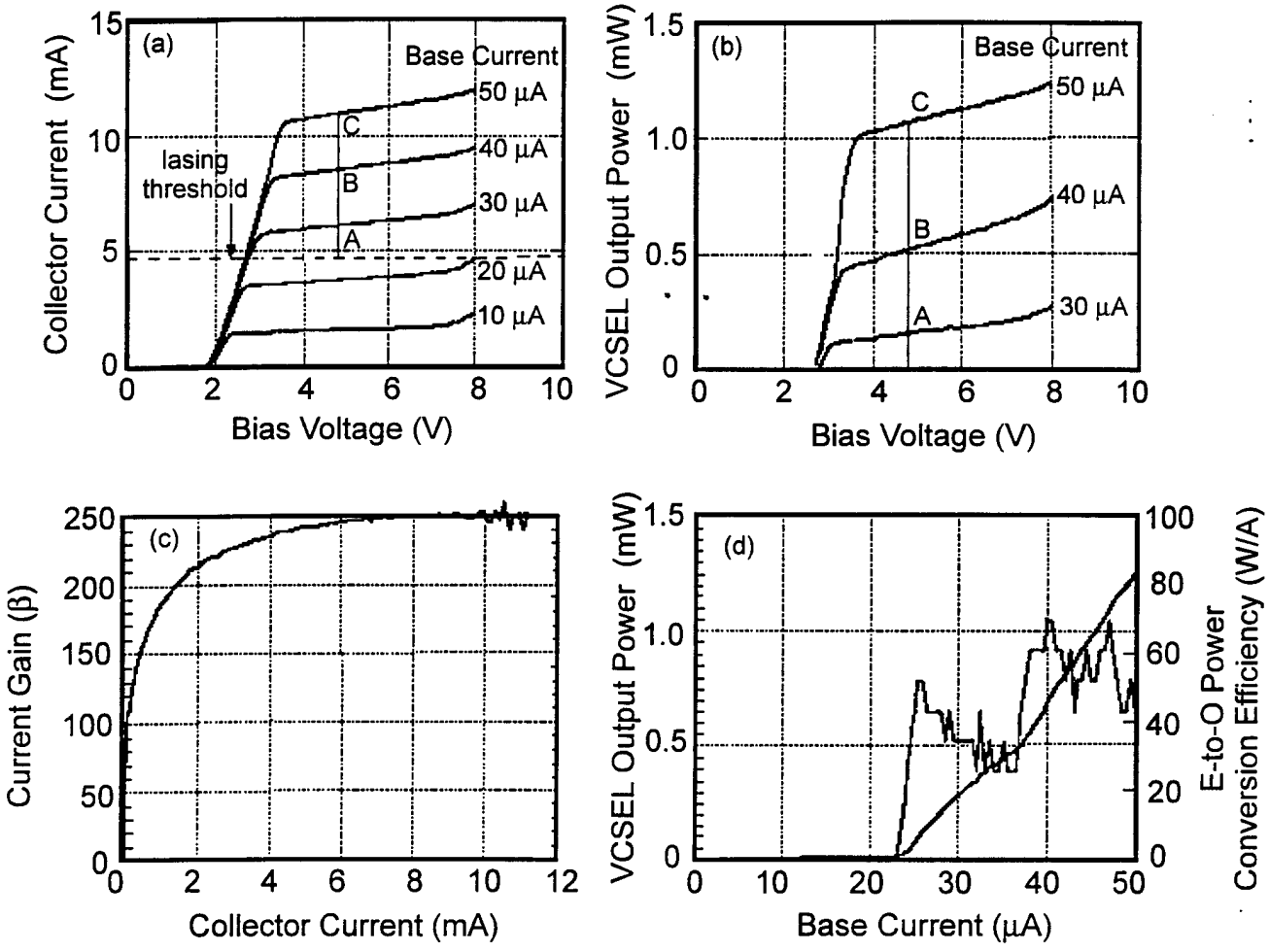

(a)
Base Current
50 μA
40 μA
30 μA
20 μA
10 μA
lasing threshold
A
B
C
Collector Current (mA)
Bias Voltage (V)
(b)
Base Current
50 μA
40 μA
30 μA
A
B
C
VCSEL Output Power (mW)
Bias Voltage (V)
(c)
Current Gain (β)
Collector Current (mA)
(d)
VCSEL Output Power (mW)
E-to-O Power Conversion Efficiency (W/A)
Base Current (μA)

Figure (13).

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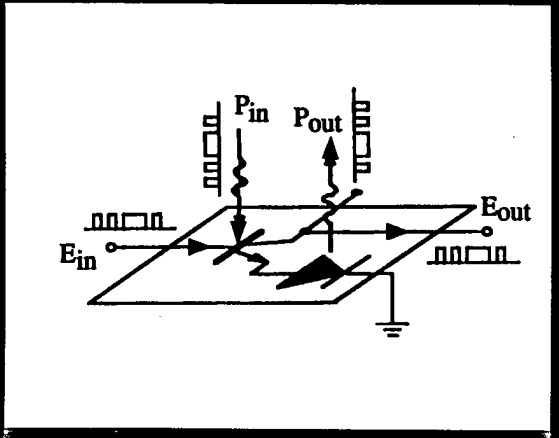
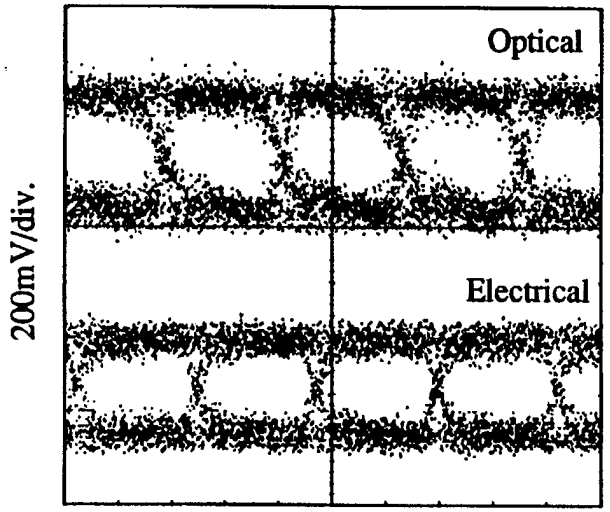
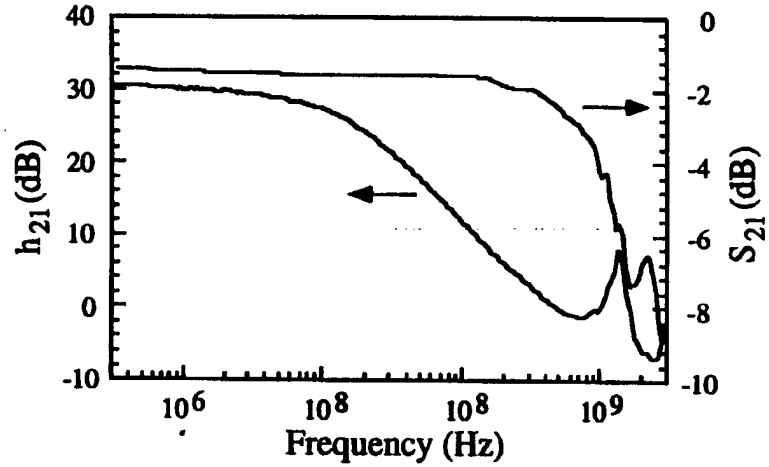
500 Mb/s ELECTRICAL TO OPTICAL MODULATION RESPONSE OF A MONOLITHIC 3-TERMINAL HPT/VCSEL SWITCH





500 Mb/s Eye Diagram

SMALL-SIGNAL MODULATION RESPONSE OF HPT



SMALL-SIGNAL MODULATION RESPONSE OF SWITCH

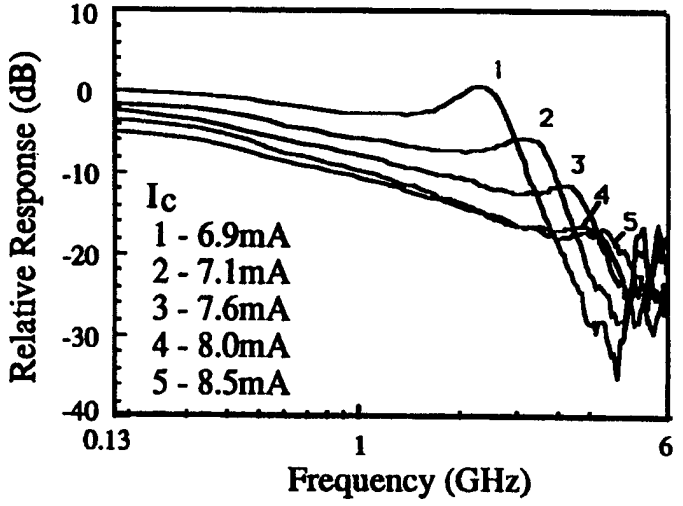


Fig. 14

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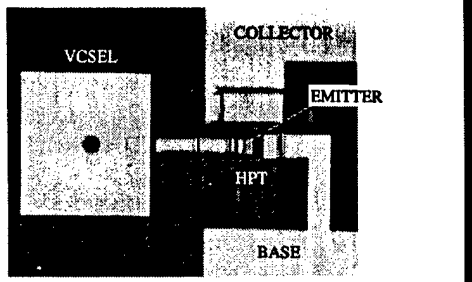
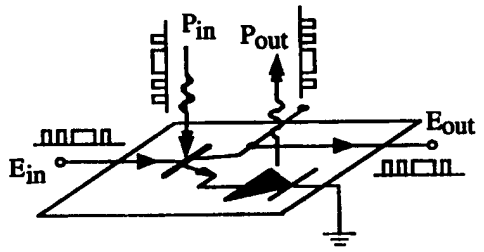
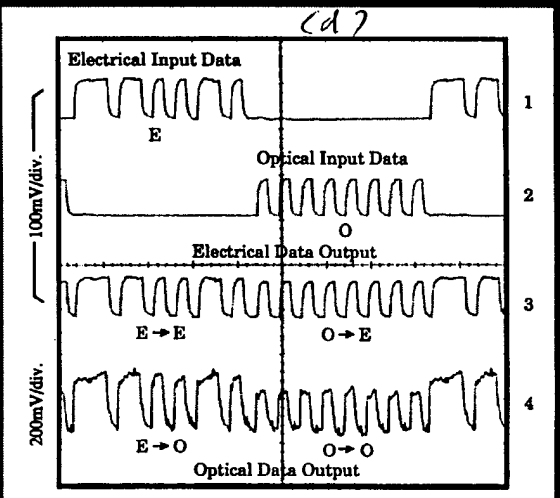
200 Mb/s MODULATION RESPONSE OF A MONOLITHIC HPT/VCSEL OPTICAL SWITCH



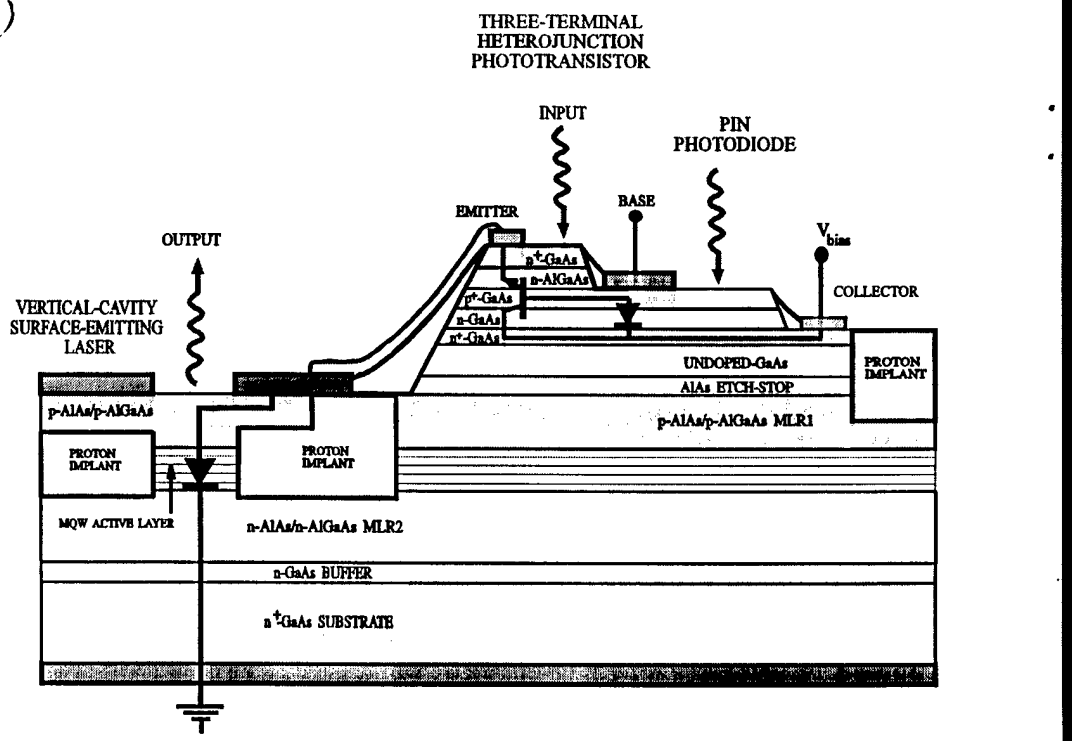
(a)



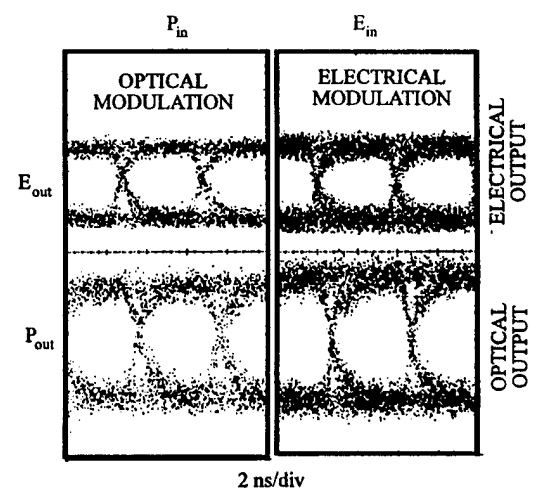
(c)



(b)



(e)



LARGE-SIGNAL MODULATION
200 MB/S EYE DIAGRAMS

FIG 15

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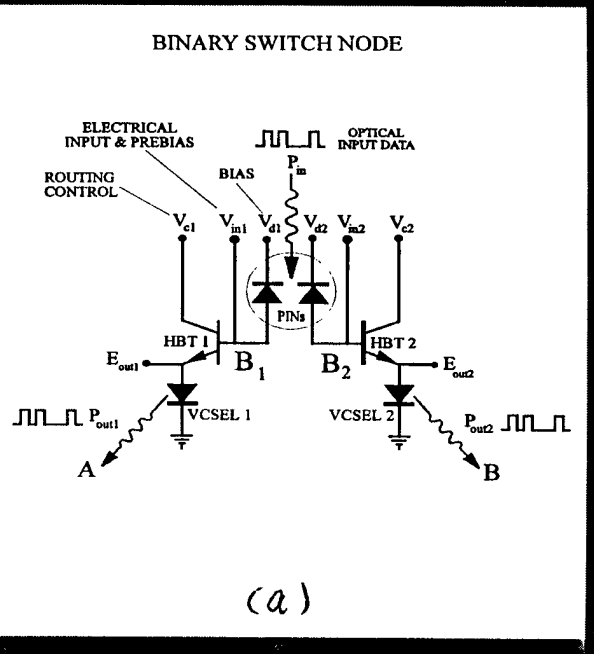
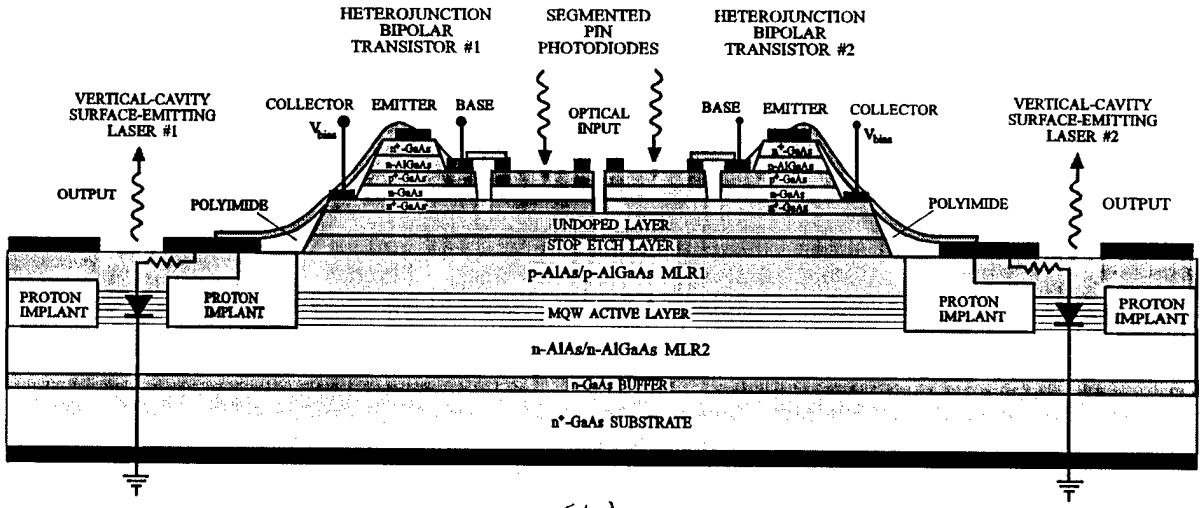
University of New Mexico, Center for High Technology Materials

INTEGRATED PIN/HBT/VCSEL OPTICAL ROUTING SWITCH

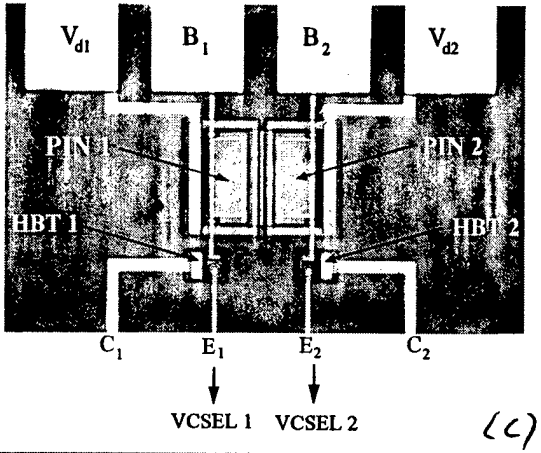


(a)

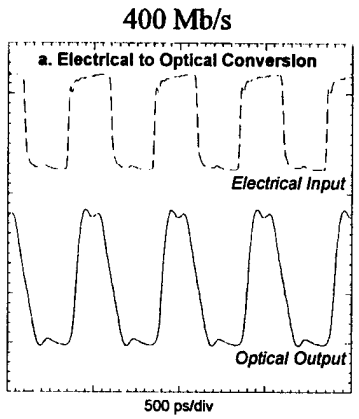


(b)

SWITCH LAY-OUT

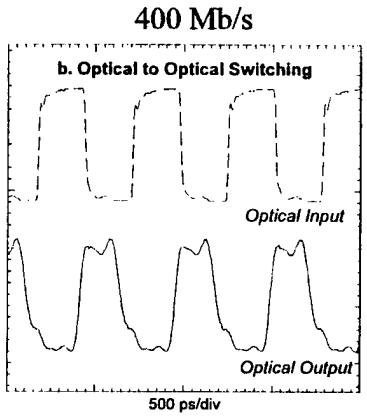


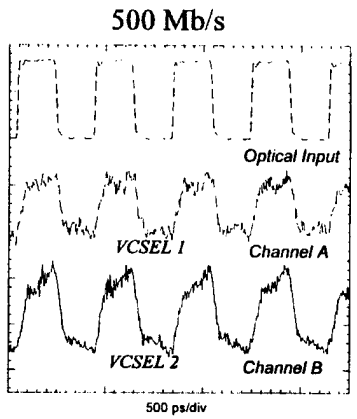
(c)



ELECTRICAL-TO-OPTICAL

(d)





OUTICAL SWITCHING, ROUTING AND FAN-OUT

(e)

(f)

Fig. 16

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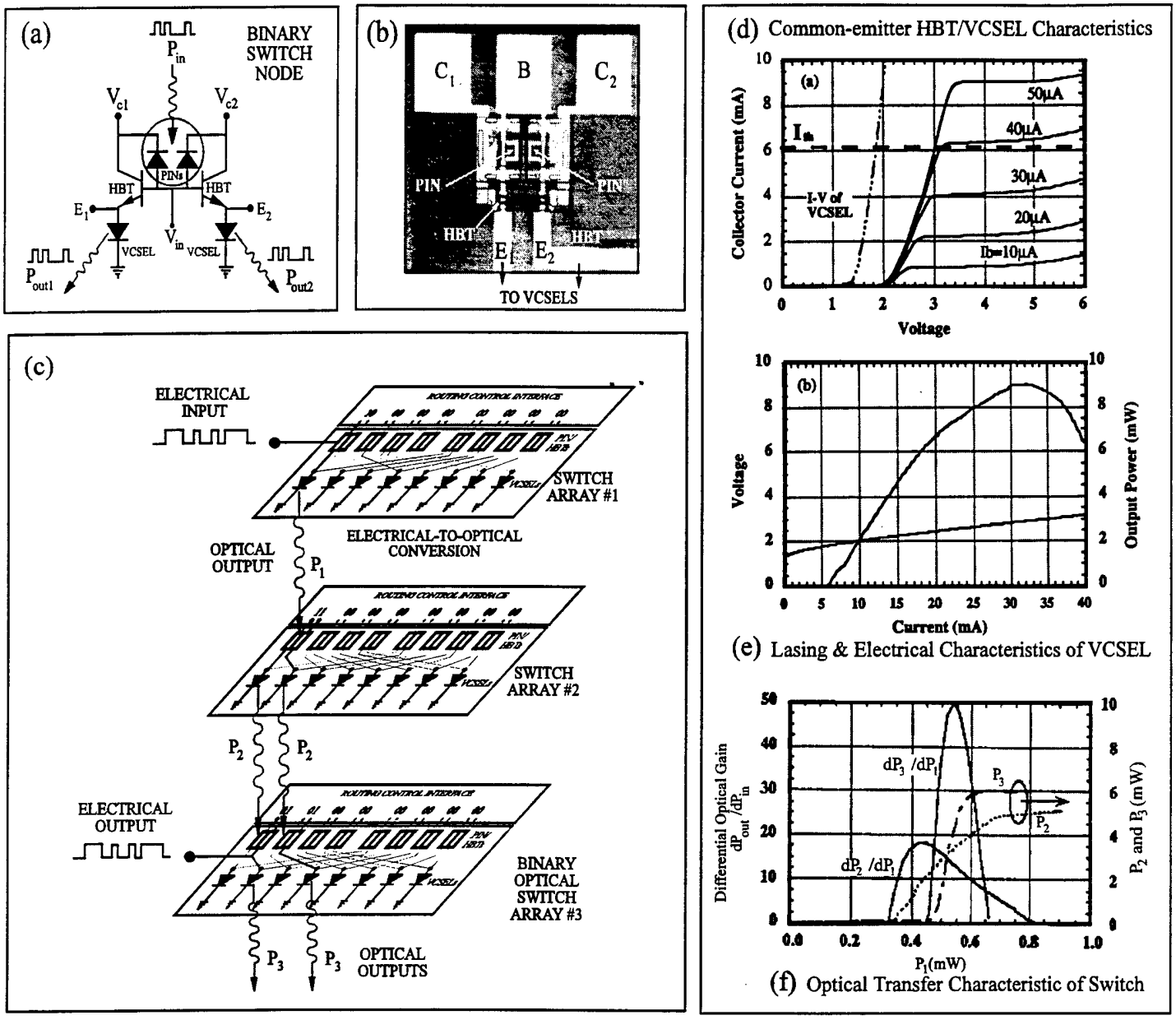

Figure 17. (a) The circuit design, and (b) layout of a reconfigurable binary PIN/HBT/VCSEL optical routing switch. (c) shows an optically-cascaded, multi-stage switching network using arrays of binary switches to perform optical routing functions. (d) shows the common-emitter characteristics of the HBT, (e) shows the lasing and electrical characteristics of the VCSEL, while (f) shows the differential optical gain of each of the two stages under optically cascaded dc switching operation.

HIGH SPEED SWITCHES FOR RECONFIGURABLE OPTICAL LOGIC GATE ARRAYS AND INTERCONNECTS

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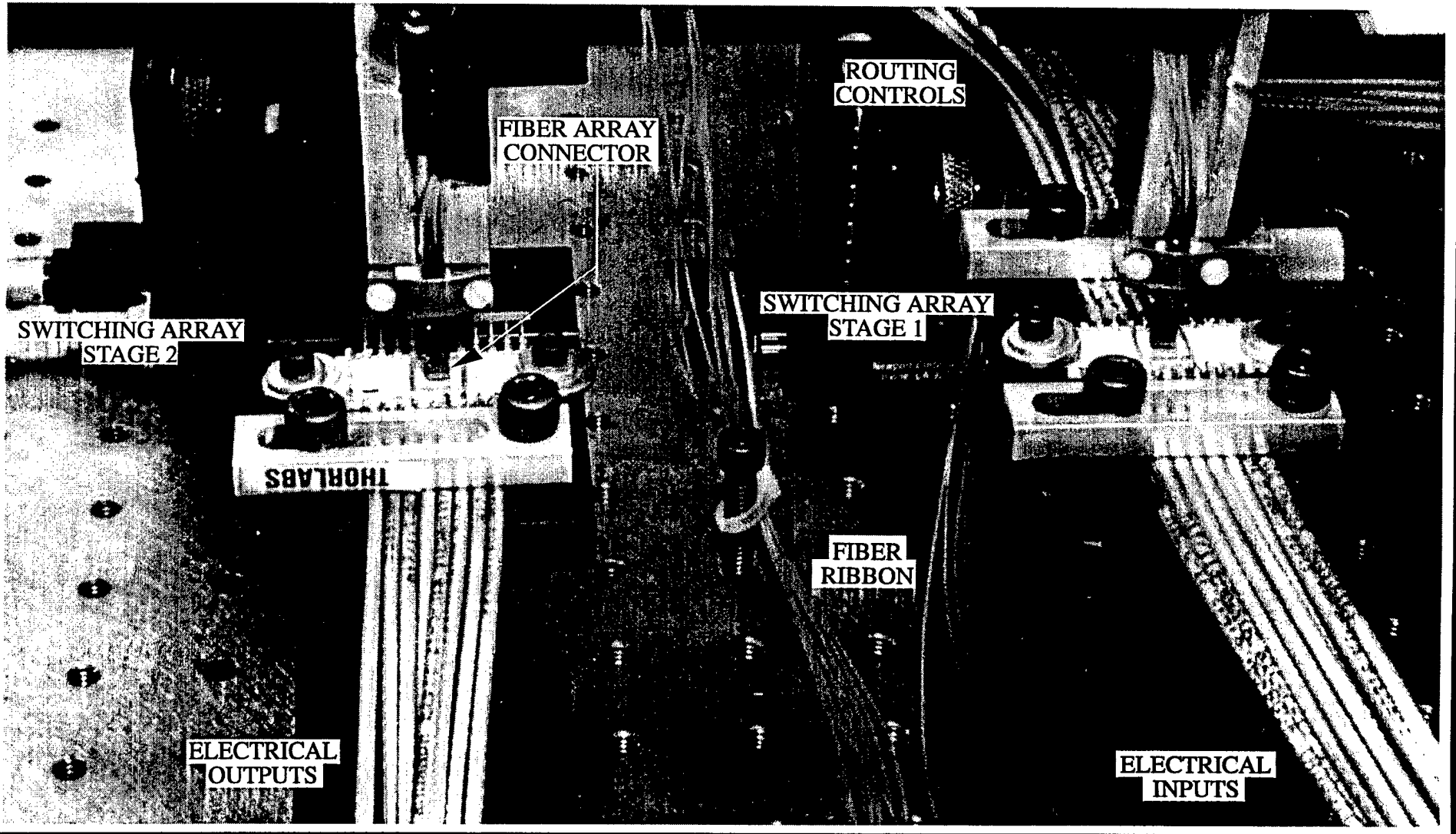
8X8 RECONFIGURABLE OPTICAL INTERCONNECT



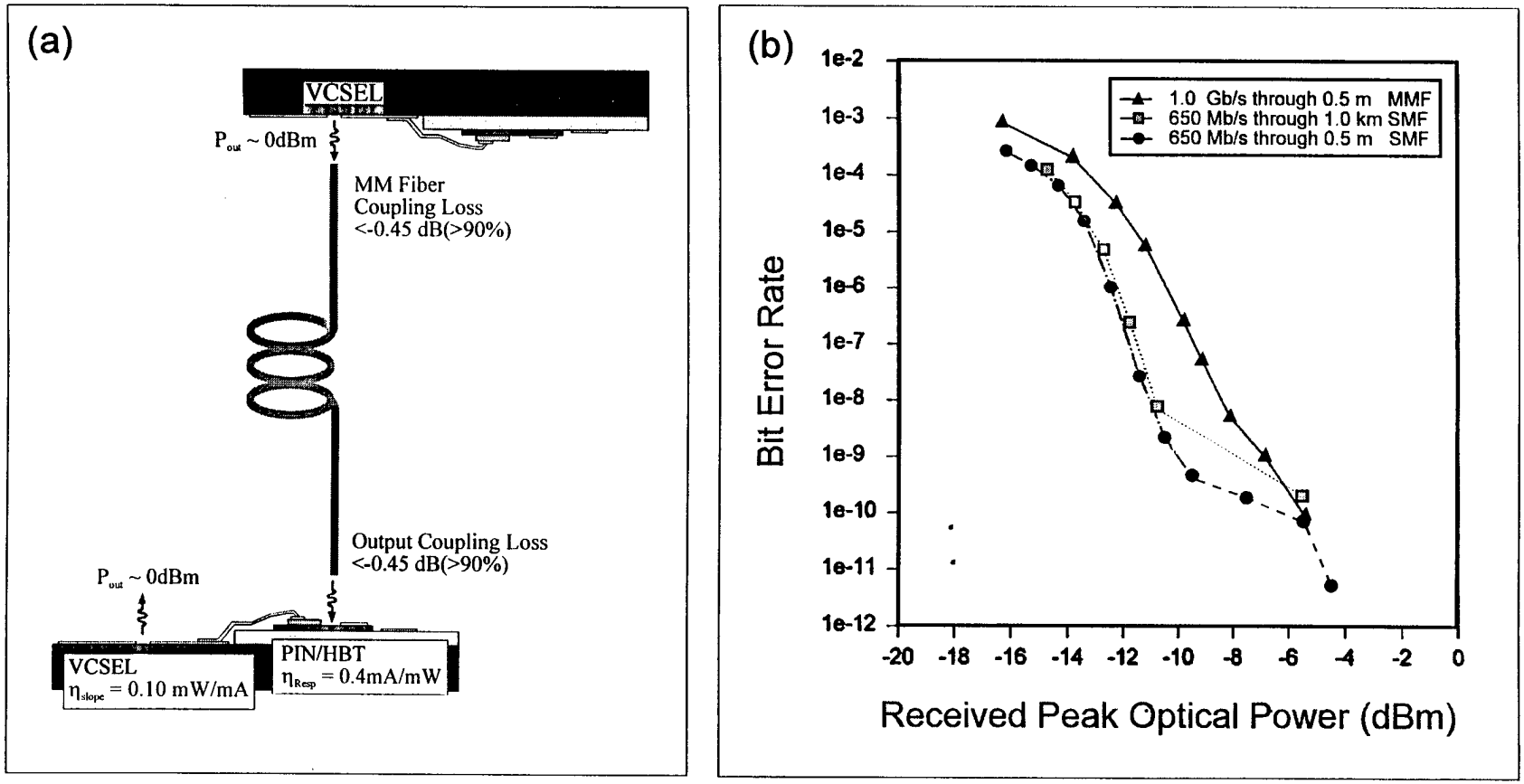

(a)
VCSEL
P_{out} ~ 0dBm
MM Fiber
Coupling Loss
<-0.45 dB(>90%)
Output Coupling Loss
<-0.45 dB(>90%)
P_{out} ~ 0dBm
VCSEL
η_{slope} = 0.10 mW/mA
PIN/HBT
η_{Resp} = 0.4mA/mW
(b)
Bit Error Rate
1e-2
1e-3
1e-4
1e-5
1e-6
1e-7
1e-8
1e-9
1e-10
1e-11
1e-12
-20
-18
-16
-14
-12
-10
-8
-6
-4
-2
0
Received Peak Optical Power (dBm)
1.0 Gb/s through 0.5 m MMF
650 Mb/s through 1.0 km SMF
650 Mb/s through 0.5 m SMF

Figure (19).

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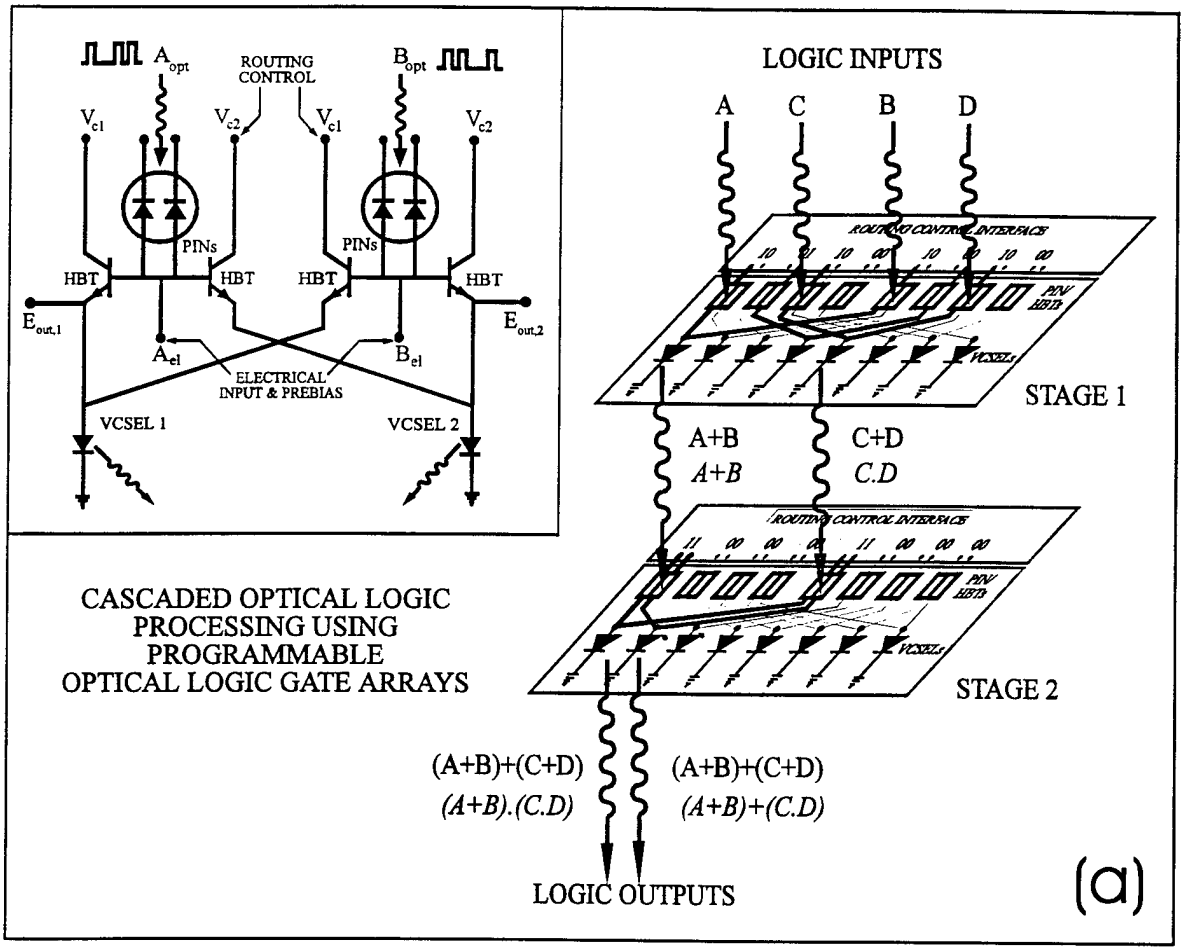
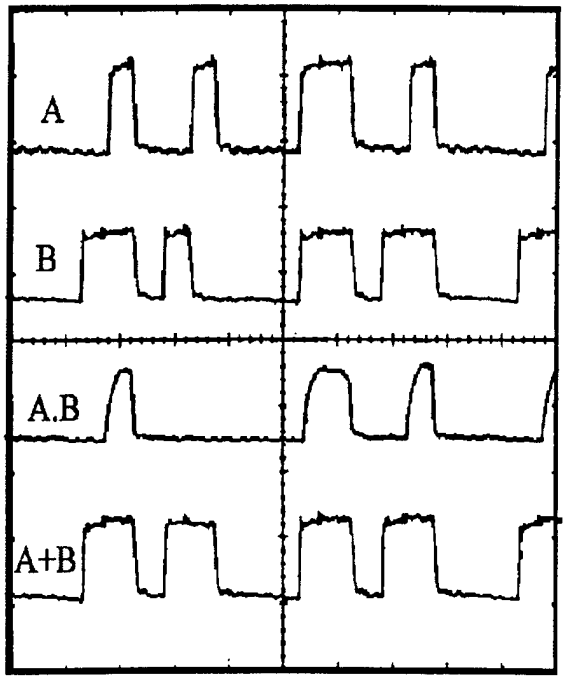


CASCADED OPTICAL LOGIC PROCESSING USING PROGRAMMABLE OPTICAL LOGIC GATE ARRAYS

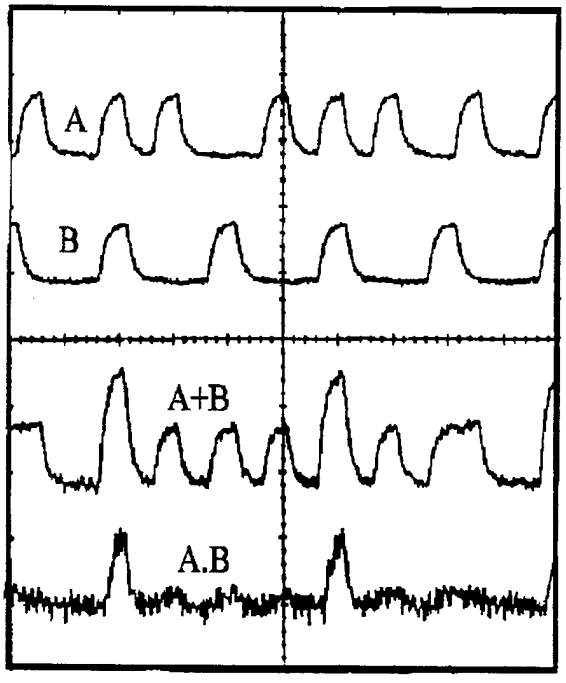
ELECTRICAL IN - OPTICAL OUT



20 ns/div

(b) ELECTRICAL LOGIC INPUTS OPTICAL LOGIC OUTPUT

OPTICAL IN - OPTICAL OUT



20 ns/div

(c) OPTICAL LOGIC INPUTS OPTICAL LOGIC OUTPUT

FIGURE 20

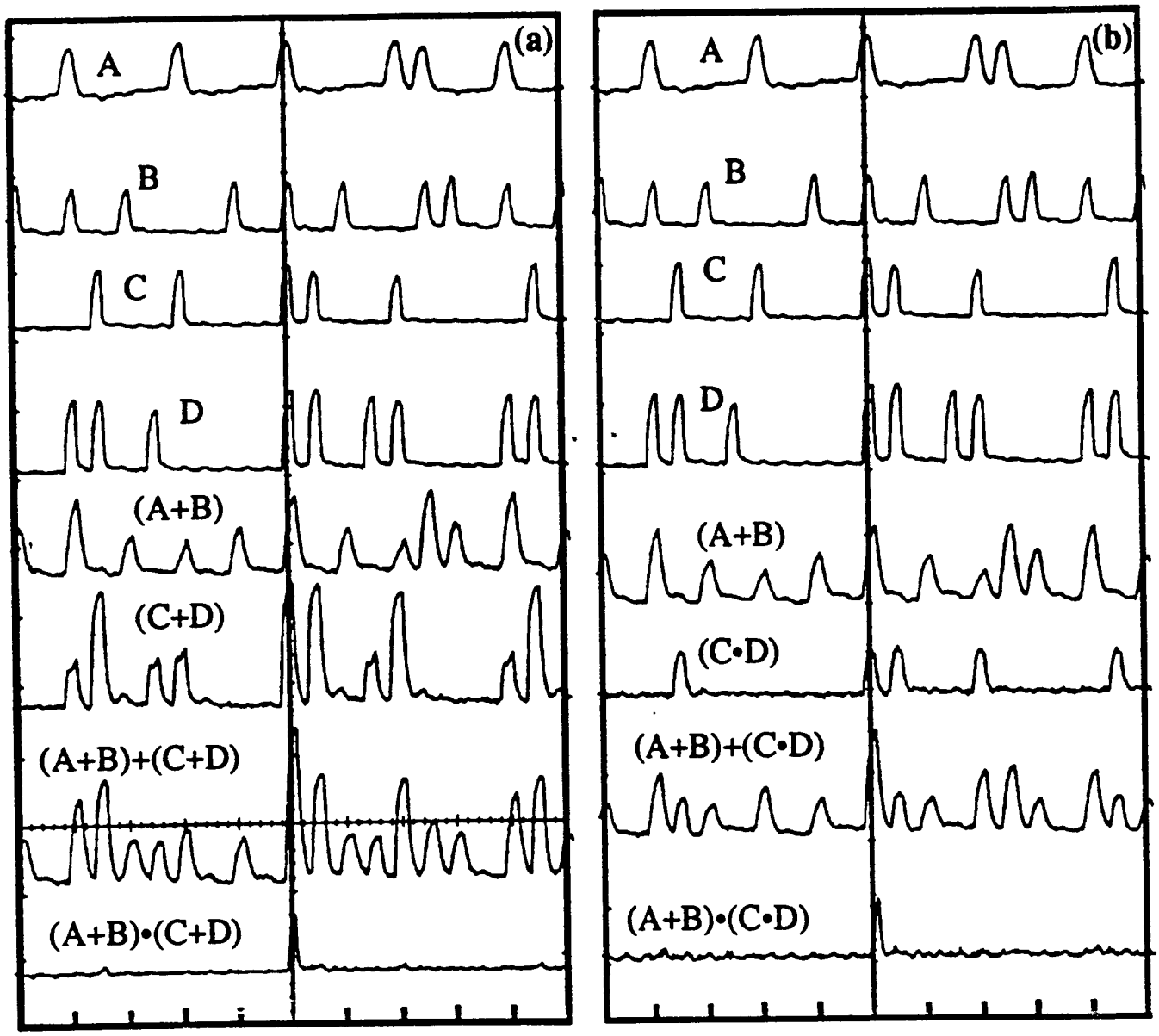

(a)
A
B
C
D
(A+B)
(C+D)
(A+B)+(C+D)
(A+B)•(C+D)
200ns/div
(b)
A
B
C
D
(A+B)
(C•D)
(A+B)+(C•D)
(A+B)•(C•D)
200ns/div

FIG. 21

HIGH SPEED SWITCHES FOR RECONFIGURABLE OPTICAL LOGIC GATE ARRAYS AND INTERCONNECTS

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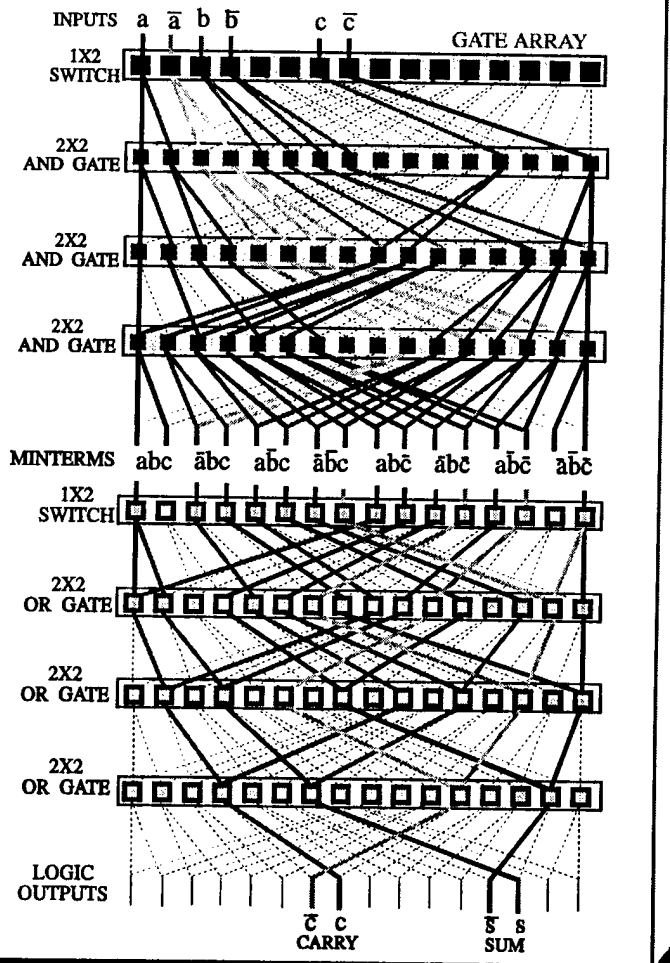
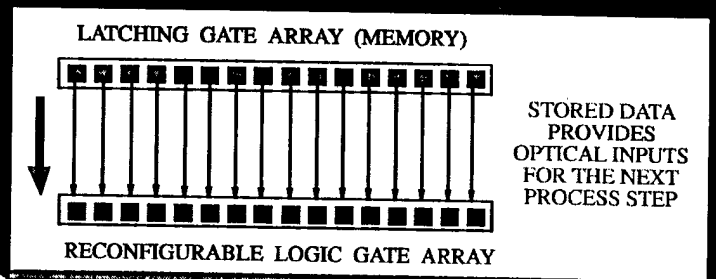
MTO

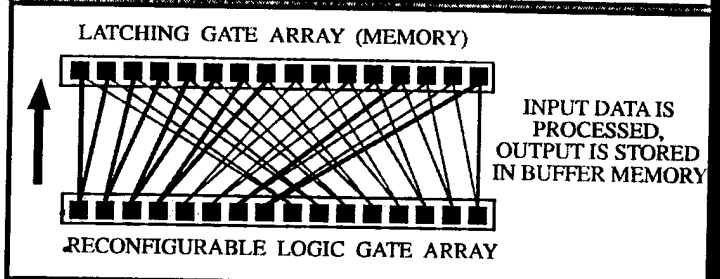
CASCADED MULTI-STAGE PROGRAMMABLE LOGIC GATE ARRAY

THE FUNCTION, OUTPUT PATH, AND FAN-OUT OF EACH GATE IN AN ARRAY ARE INDIVIDUALLY PROGRAMMABLE



PROGRAMMABILITY OF THE LOGIC ARRAY ALLOWS THE ENTIRE MULTI-STAGE PROCESS SEQUENCE TO BE FOLDED INTO A TWO-CHIP PLGA





OPTICALLY-FOLDED TWO-CHIP PROGRAMMABLE LOGIC GATE ARRAY